Advanced System-in-Package design services: benefits and trades-off

By Luc Engrand

The System-in-Package (SiP) concept can be defined as of integrating several heterogenous components like semiconductor and passive devices into a single package or miniaturized module. This allows for extremely rapid and low cost development cycles.

This article will highlight the key benefits of having a SiP implementation especially for RF applications and how a company like Insight SiP can contribute to its customer success through Full-Turnkey Design Services while applying its own advanced packaging design methodology.

The SiP approach to RF system integration has become essential to the miniaturization roadmap. Despite a long term tendency to integrate more and more functions within a single die (System-On-Chip concept) the never ending increase in complexity for small personal devices continues to drive the use of SiP to make complete systems. RF SiP can be realized using several types of technologies which are specific to each selected manufacturing supplier; therefore the SiP implementation will need to be tailored to the specific design rules based on different materials, physical dispositions and properties.

It is essential that the design house partner can combine its RF know-how with the unique ability to embed functions within the package irrespective of the packaging/assembly technology: organic substrates (BT, FR4...), multi-layer ceramic substrates (LTCC, HTCC, Thick film...), wire-bonding, flip-chip or thin film Integrated Passive Devices (IPD) on silicon or glass.

Two examples of SiP products developed by Insight SiP are shown in figure 1.

The addition of ultra-miniature antennas to the RF SiP to create a so called “Antenna in Package” product (AiP) has been a fundamental part of the Advanced Technology Development. This technology has been successfully implemented in wireless products for Bluetooth Low Energy (BLE) and Ultra-Wide-Band (UWB) applications.

Why SiP approach addresses today’s challenge

With the massive adoption of consumer electronic products embedding more and more complex functions, it is important that new devices meet low power, smaller aspect-ratio requirements while remaining cost competitive. Therefore engineers and product development teams are facing the several challenges including the fact that shrinking nodes no longer necessarily reduce the cost per transistor (from 65nm onwards), SoC development time, NRE and risk of failure are increasing with every node, and high growth markets (IoT, Automotive...) demand cost-effective integration of heterogeneous functions (Memory, MCU, GPU, Analogue, RF, MEMS, CIS...) in a small space.

Lower power has replaced higher speed as the most important IC feature and devices need to be wirelessly connected through existing RF protocols (eg cellular) or emerging networks (e.g. LPWAN like LoRa, SigFox, LTE-M, NB-IoT). Only the SiP approach helps in meeting those paradigms because the system partitioning offers More-than-Moore capabilities, the modularity of SiPs simplifies adding heterogeneous functions to digital SoCs and combining multiple dies in one IC package will reduce power dissipation by 3 -10 X, versus mounting individually packaged dies onto a Printed Circuit Board.

Multi-die IC design and manufacturing flows are maturing, reducing NRE and development times making SiPs economical also for low to medium volumes. IDM’s and fabless IC vendors who have announced many interposer-based IC, are now ramping up production and have more such 2.5D-IC designs in progress. Major open foundries like TSMC have invested significantly into their own multi-die packaging line and most big OSAT companies have developed and offer WLP solutions. What’s more, several EDA vendors offer user friendly modelling- and design tools to minimize development time and risk while reducing multi-die IC unit cost.

According to TechSearch International, 13.3 Billion SiPs were shipped in 2015. Almost 70% of the units were RF and connectivity modules as shown in figure 2.

Today’s high-performance semiconductor applications are primarily bandwidth and power limited. Samsung, IBM, HiSilicon, Nvidia and others have already demonstrated the benefits of combining several dies, stacked or side by side on an interposer. Compared to individual ICs on a PCB, very short die-to-die connections and very wide busses enable significant performance increases and, at the same time, power reductions. Today’s fastest growing semiconductor opportunities (Mobile Devices, Automotive, and IoT Nodes) need a multitude of heterogeneous functions, to interact with the world around them. Combining multiple heterogeneous dies and sensors in a SiP meets their space, power and cost constraints.

Advanced design methodology for seamless integration

To address the rapid demand of RF and consumer SiP type products, Insight SiP has developed a proprietary advanced design methodology combining electromagnetic simulations (3D EM) together with circuit level simulation and optimization. Running exhaustive front-end EM simulation as an overall strat-
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In the identification of a SiP design house partner, industrialisation and production supports are key enablers. A company like Insight SiP has access to world leaders design rules for each SiP manufacturing technology and packaging. This allows selection of the most effective combination of process and production for each custom project.

It is essential, especially for complex RF systems, to have a close relationship with the different OSAT manufacturing partners, and Insight SiP has established a strong cooperation with major vendors like Amkor, AT&S, Tong-Hsing, Kyocera, SPIL… This is a key benefit during the industrialisation phase to secure production supply and yield improvement (e.g. RF/Antenna tuning during the ramp-up phase).