

Trusted Resource for the Working RF Engineer



[Components]

System-In-Package Design Approach Promotes Portability

Diana Moncoquit | July 2010

Copyright © 2010 Penton Media, Inc., All rights reserved.
Printing of this document is for personal use only.



Advances in system-in-package (SiP) technology have made possible smaller circuits with increased functionality. Yet SiP solutions are not widespread because of a lack of design automation and portability. By using a design strategy that combines circuit simulation tools with electromagnetic (EM) design software, however, SiP designs can be created in stages from schematic representations to full three-dimensional (3D) EM layouts. Such designs promise true portability across a number of different foundries and circuit fabrication facilities.

The first step in this design methodology is to create a range of parameterized mechanical objects for a given SiP technology, such as low-temperature-co-fired-ceramic (LTCC) substrates. These objects allow the creation of simple RF functions, such as a capacitor (C) or inductor (L). The second step is to couple the technology file for the target process to the mechanical objects. With a series of batch-based EM simulations of the mechanical objects within the desired technology-file framework, data is created for a lookup-table (LUT)-based model for each component (L, C, or more complex resonator element).

This process allows for the creation of a set of project- and technology-related schematic objects that can be optimized to produce the required RF functionality. Simulations using these models can be carried out in both the frequency and time domains. At this level of the design, circuit optimization is carried out to determine the parameters of the schematic/mechanical object. This process is quite similar to that carried out in semiconductor design using library-based objects.

The third step of the process is to create complete sections of the physical layout with optimized mechanical objects. A closed-loop iterative process is used to obtain a final layout, which has the same electrical performance as the sum of the modeled portions. At this stage, the approach compensates for the coupling effects between blocks. The mechanical objects can therefore be placed close together without any risk of causing unseen effects. As a result, the designs created by this method are more compact than those using a "P cell" approach with large keep-out zones to avoid coupling.

RF SiPs can be realized using a multitude of technologies. For each technology, suppliers offer different materials, physical dispositions, and properties that require circuit layouts to be optimized to that technology. A given supplier's process is characterized by a technology file that describes the material parameters and physical disposition between the dielectric and metallic layers. [Figure 1](#) shows a typical technology file for LTCC.

Most SiP design methodologies, which include integrated passive components, rely on fixed libraries of components. These libraries are based on particular substrate supplier and stackup. When high volumes are involved, however, it should be possible to source an SiP from at least two independent manufacturers. The methodology discussed here is based on a user-extendable library of mechanical objects. The electrical models for those objects are created automatically for a given stack-up and/or technology. Thus, any design initially developed for one supplier can easily be re-tuned for an alternative source. The second manufacturer can have a completely separate set of electro-mechanical parameters (stackup, dielectric constant, layer thickness, loss factors, metal types) and may even use an alternative technology.

In this supplier-independent SiP design approach, mechanical objects do not have a direct link to the material properties. Nor do they have a direct connection to the vertical stack of the particular technology and supplier that is to be used. These objects can therefore be re-used if a design is transferred between two suppliers. [Figure 2](#) shows a somewhat complex LTCC mechanical object that consists of a pair of coupled resonators. For these resonators, both the resonant frequency and coupling are controlled by mechanical parameters.

The second step of the methodology is very easy to repeat with a new technology file, facilitating design transfer between suppliers and technologies. In order to redesign for an alternative supplier using the same technology, the process employs the same mechanical objects with a new set of technology values. This process starts from the same basic schematic and simply re-optimizes the object parameters to compensate for the new physical and mechanical parameters. The final EM closed-loop process is then carried out to create a layout for the new supplier.

To change from one technology to another, equivalent mechanical objects that have similar functions in both technologies must be developed. The same basic schematic is used and the schematic/mechanical objects are swapped. Thereafter, the process is similar to the normal design flow.

To illustrate how this methodology works, consider the transfer of a Bluetooth filter design between LTCC suppliers. The three-pole, one-zero filter is designed to fit under the active components in a Bluetooth module. Although the filter was originally designed for a specific LTCC foundry, it was successfully transferred to a second foundry. The filter is designed using semi-distributed transmission-line resonators with resonator coupling to create a suitable frequency zero in the response.

The stacks and material properties of the two suppliers are quite different ([Fig. 3](#)). Yet the mechanical objects were converted from one stack to the other and the design process was completed rapidly. Although the two filters are quite similar, their physical dimensions are slightly different to compensate for the LTCC stack differences. The electrical performance for both realizations was similar.

Continue to page 2

Application To Antenna Design

For integrated antenna design, EM simulations were combined with circuit-level simulation and optimization. This helps to circumvent lengthy parametric studies while significantly shortening the design cycle. The methodology was used to design antennas for various applications including a quadband GSM antenna as well as a 2.4-GHz industrial, scientific, and medical (ISM)-band antenna. It also was extended to implement a challenging ultrahigh-frequency (UHF)-band antenna.

In the case of the 2.4-GHz ISM module, the antenna was originally a printed trace wiggly antenna on a printed-circuit board (PCB). The size of the antenna and the groundplane was 28.5 x 15 mm². By applying the previously mentioned technology, it was possible to integrate the module and antenna into an 8-x-12-mm² QFN-type package. In this case, the antenna takes advantage of the multilayered structure of the substrate in which it is embedded. That structure has at least a top and a bottom wiring layer. A portion of the surface area is reserved for the antenna while the remaining area is used for active- and passive-component placement/routing and groundplane.

The most challenging parameter in designing integrated antennas is the environmental impact. The environment includes different building materials for indoor and outdoor use, high-rise buildings, factories, and major highways. Simulations and validations are needed to optimize the antenna design for different environmental conditions. As an example, a wideband antenna was developed using the example methodology. As a result, the groundplane and manufacturing variations do not significantly affect the antenna performance. [Figure 4](#) compares simulated and measured S11 parameters for the 2.4-GHz antenna-in-package. [Figure 5](#) shows its radiation pattern with excellent field response in all planes.



[Planet EE Network Home](#) | [Contact Us](#) | [Editorial Calendar](#) | [Media Kit](#) | [Headlines](#) | [Site Feedback & Bugs](#)
Copyright © 2010 Penton Media, Inc., All rights reserved. Privacy