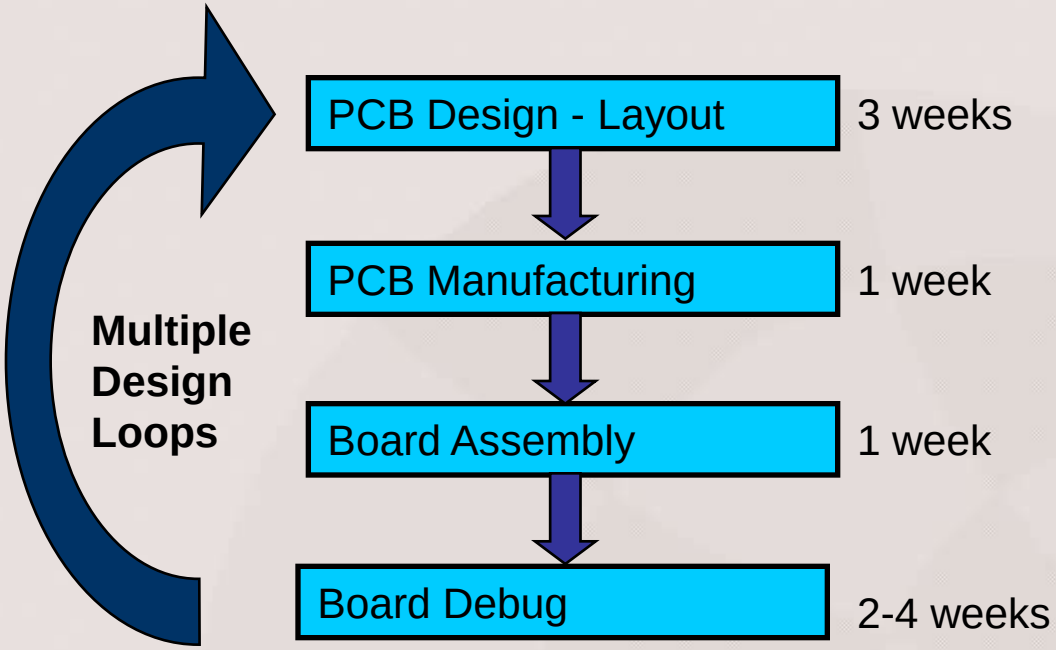
INSIGHT SIP

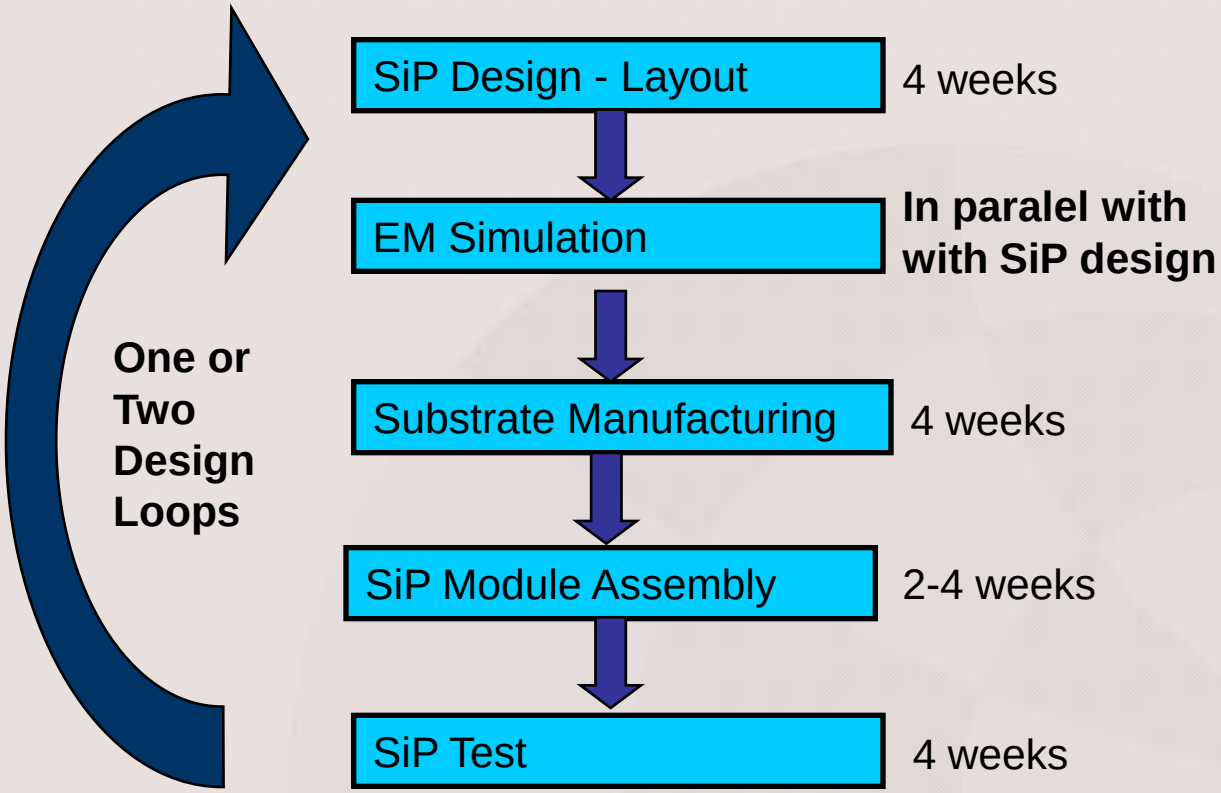
DESIGN PROCESS

SIMPLE PCB DESIGN



Board Design
Typical Lead Time for 1 loop : 7-9 weeks

SIMPLE SIP DESIGN



SiP design
Typical Lead Time for 1 loop : 14-16 weeks

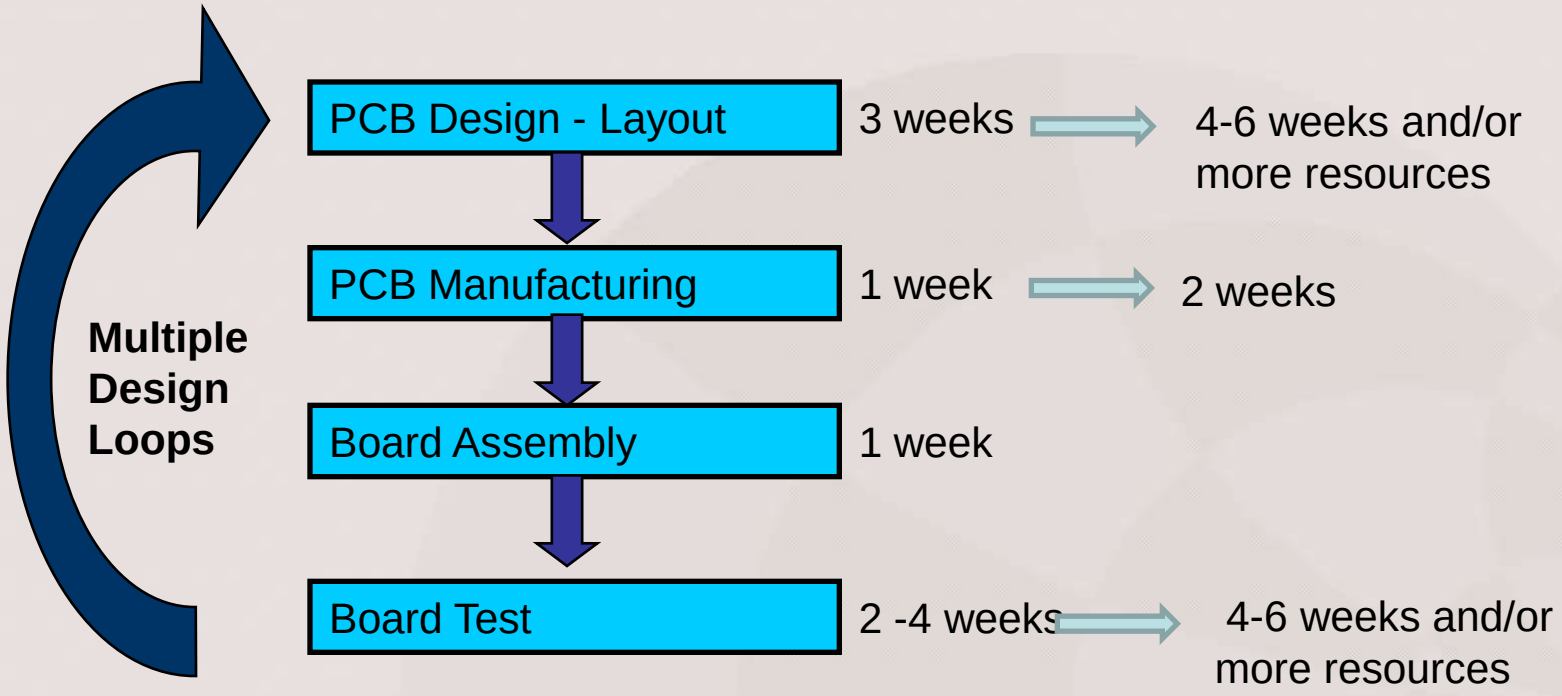
More Complex Designs

Let’s examine the situation when the design is more complex!!!

➔ More than 2 die, More than 400 connections

COMPLEX PCB DESIGN

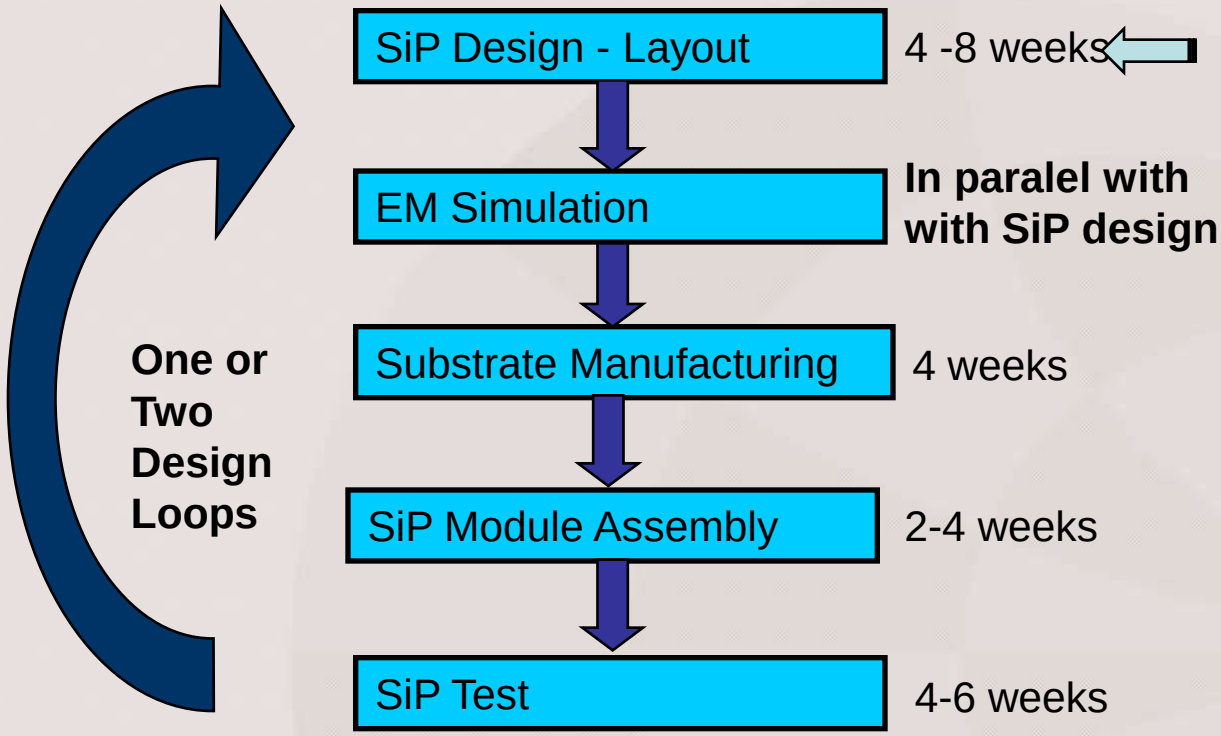
More than 5 large LGA, BGA components, More than 500 nets



Board Design
Typical Lead Time for 1 loop : 11-15 weeks

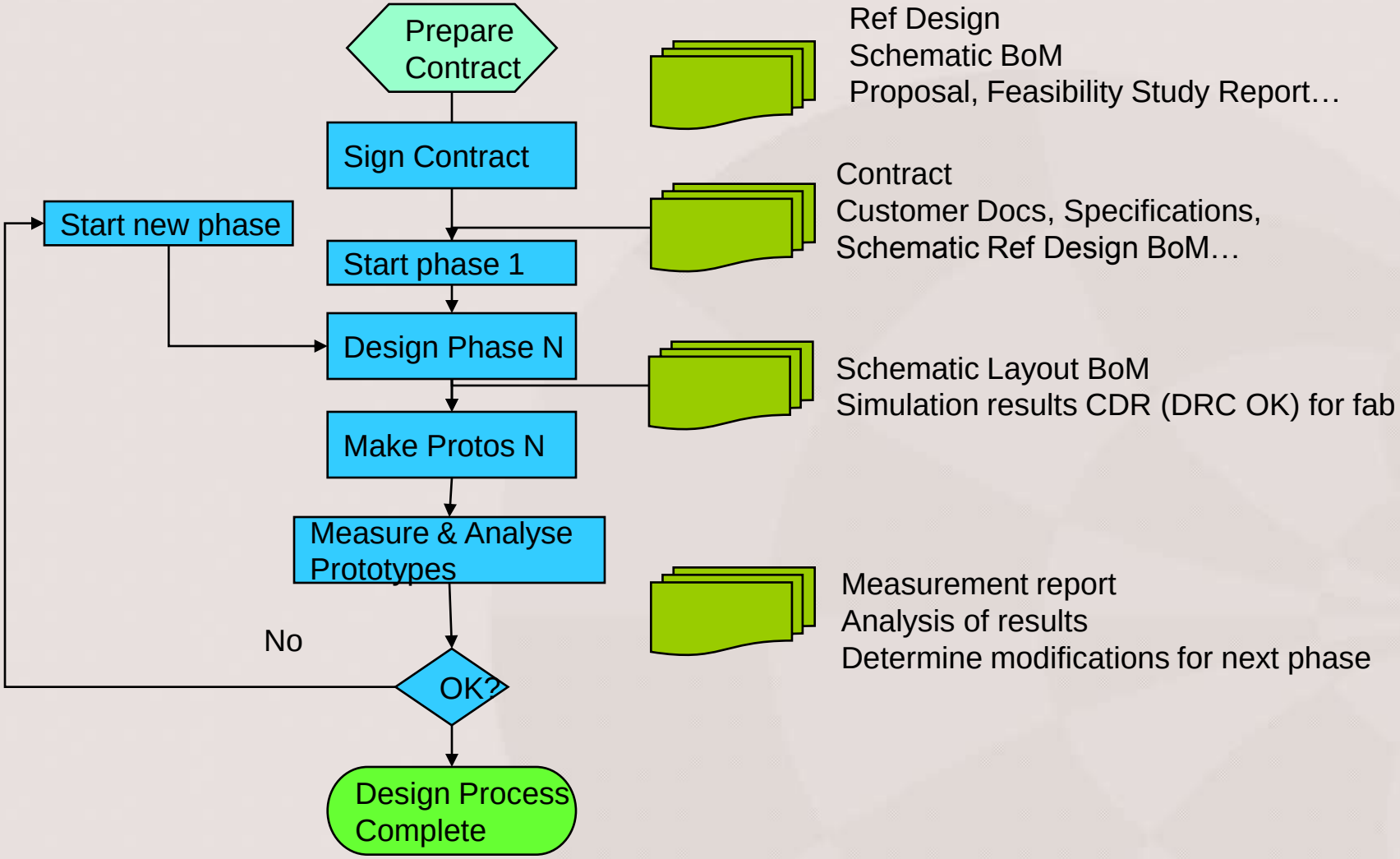
COMPLEX SIP DESIGN

More than 2 die more than 400 nets Complex RF interactions

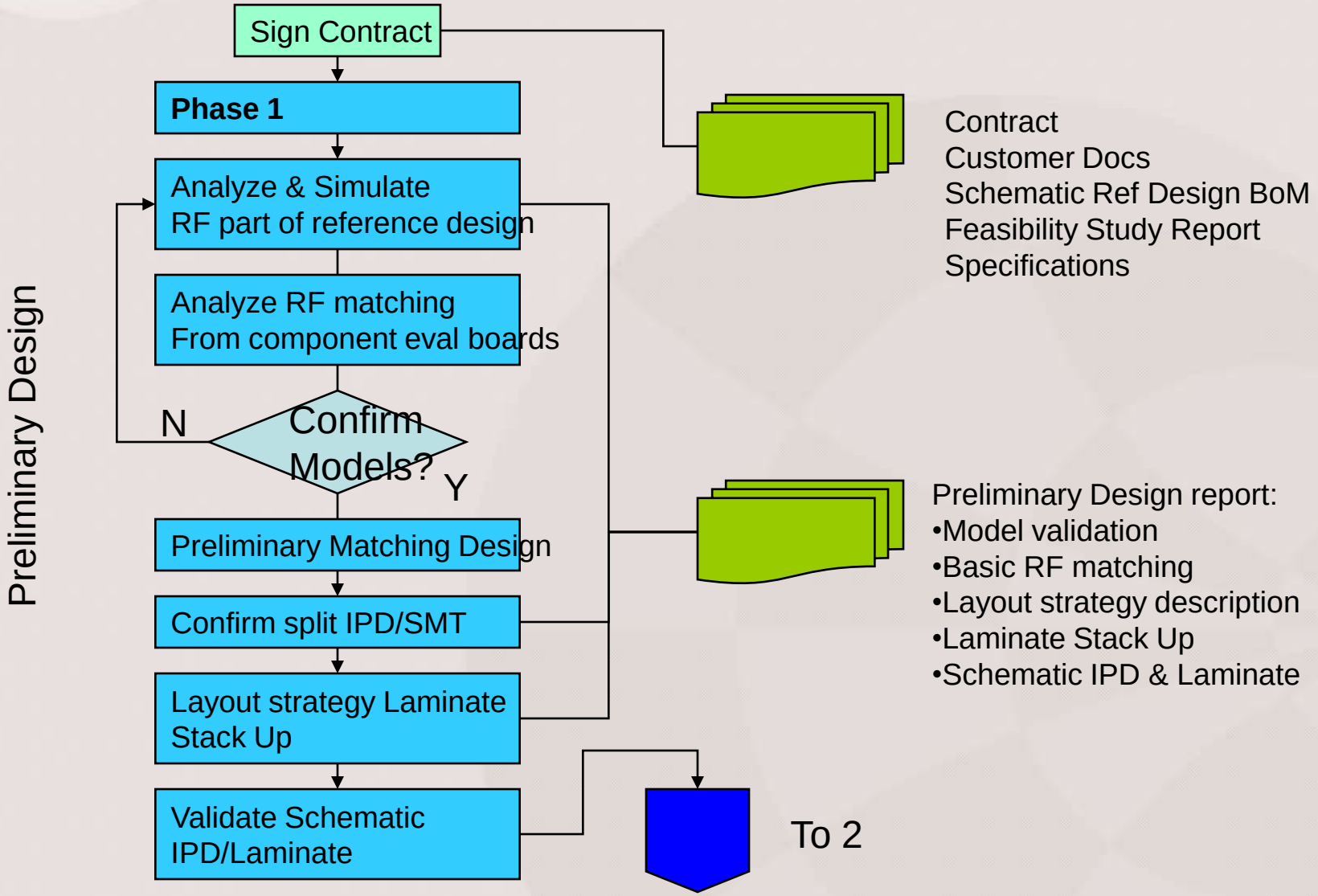


SiP design
Typical Lead Time for 1 loop : 14-22 weeks

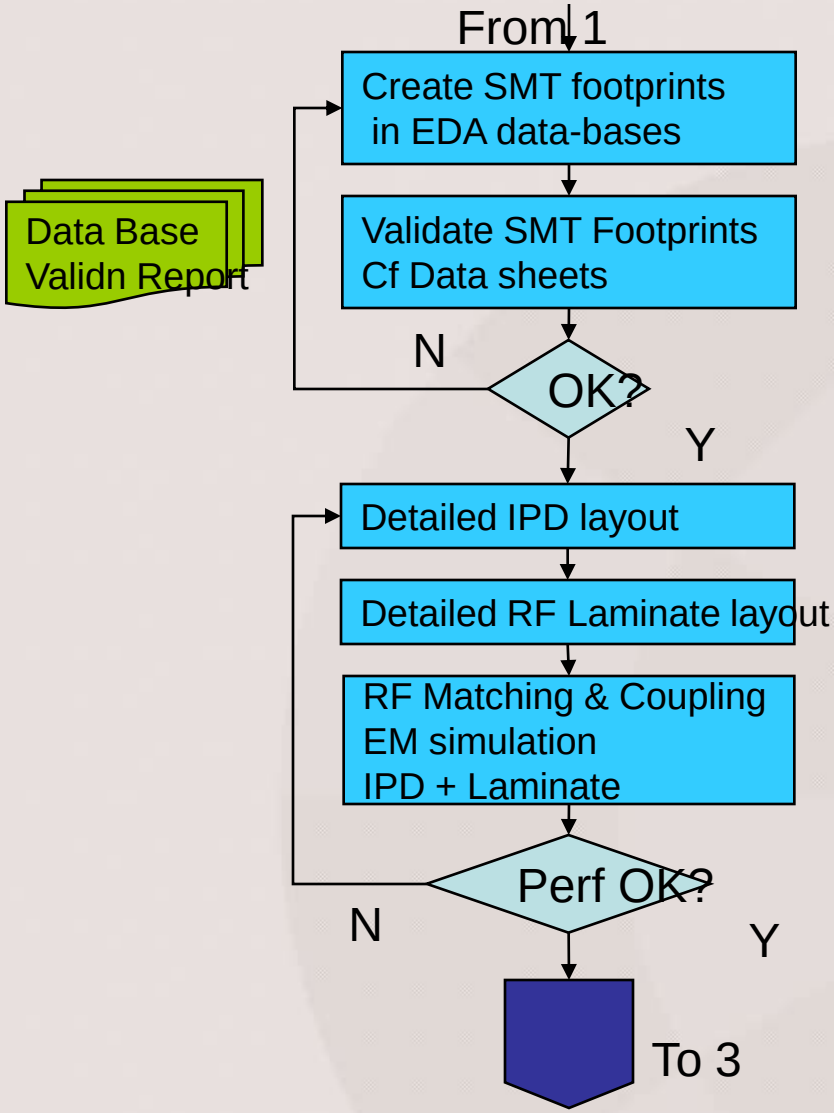
Overall Design Process



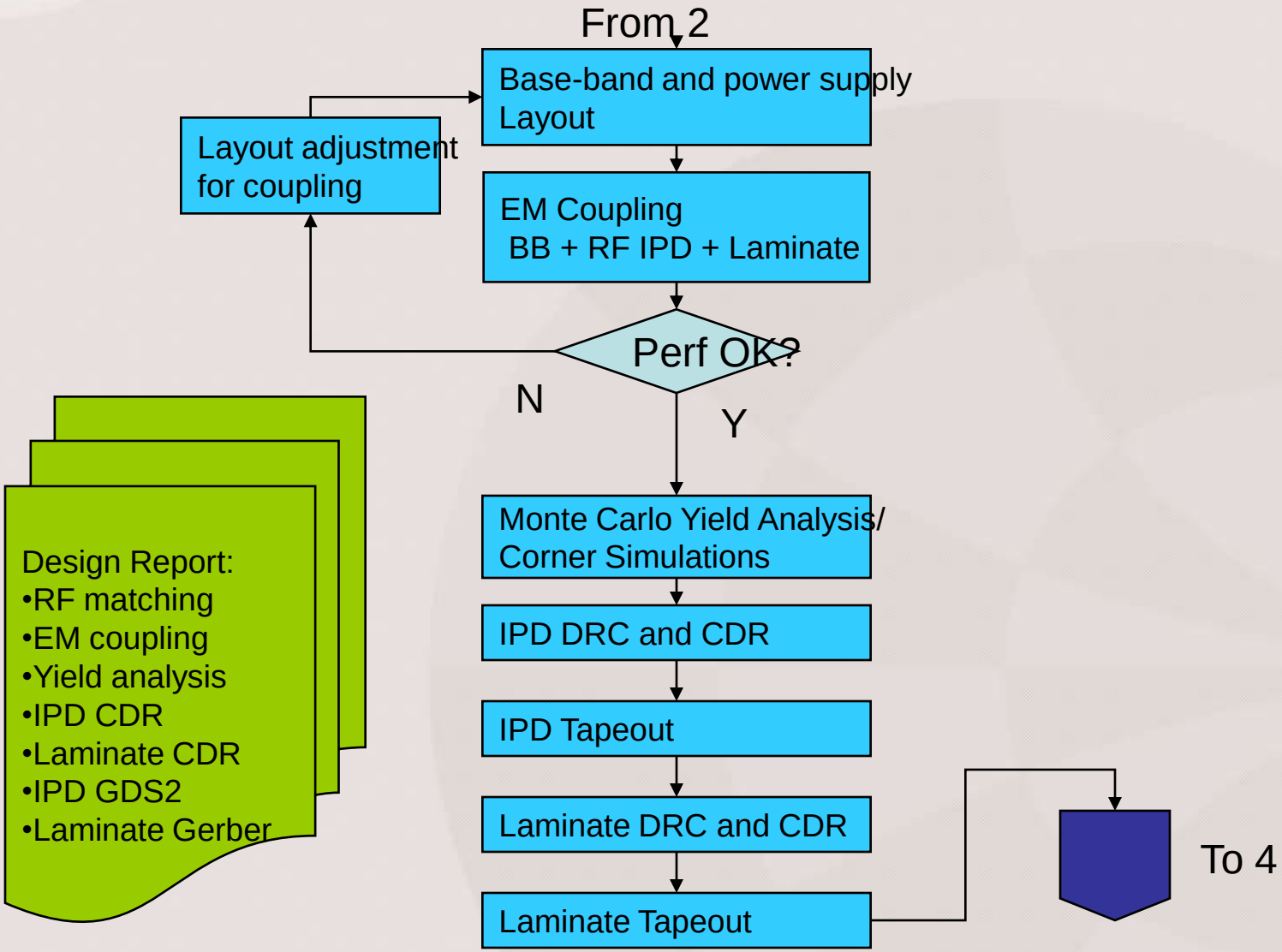
Detail Design Process 1



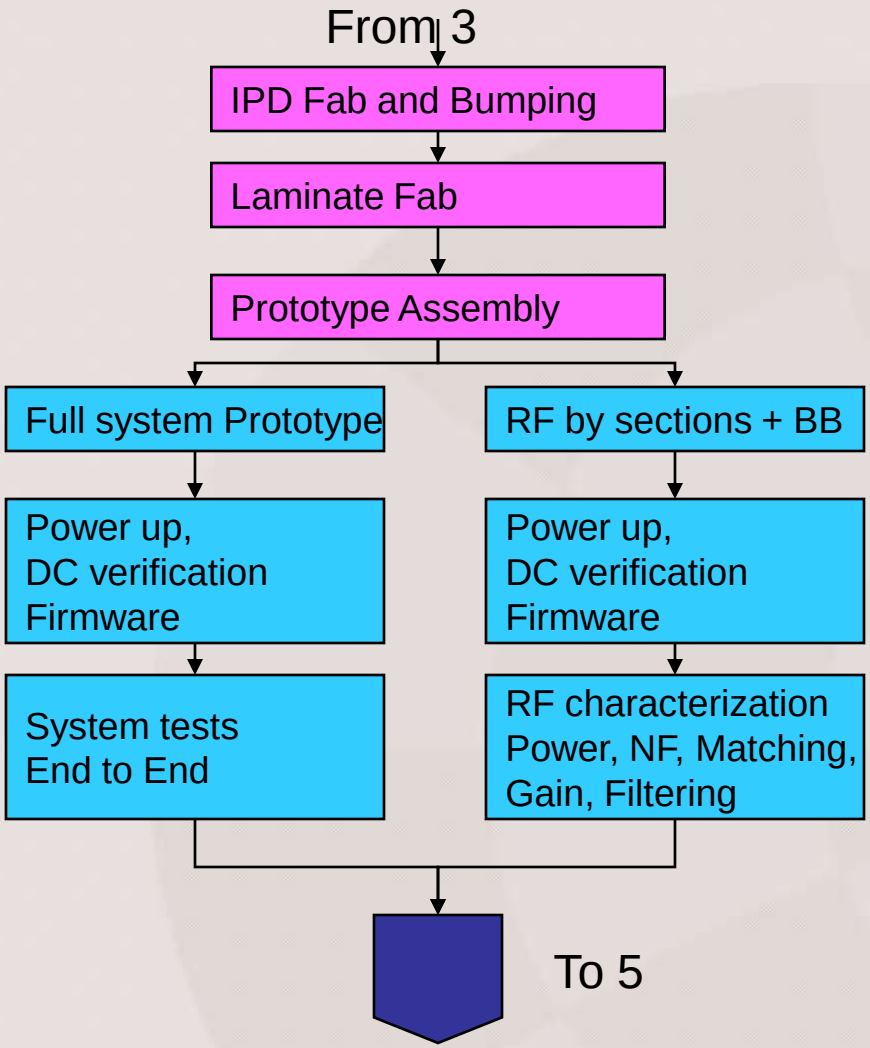
Detail Design Process 2



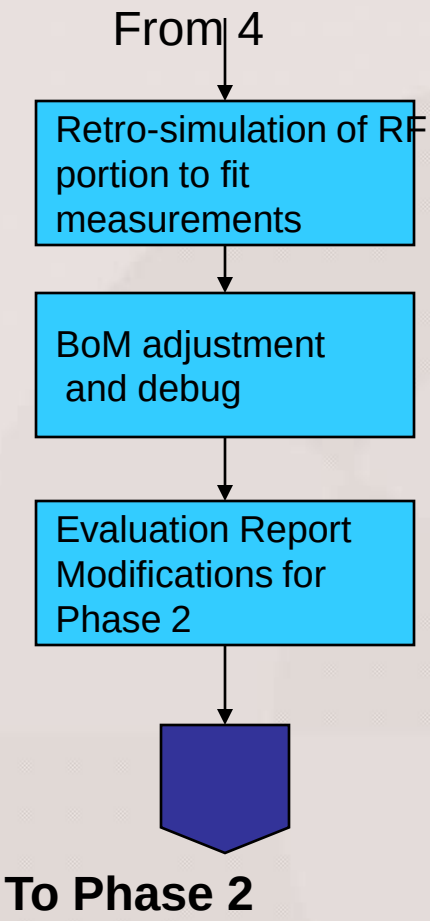
Detail Design Process 3



Detail Design Process 4

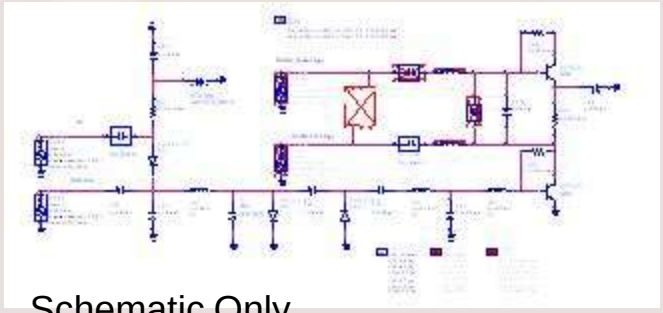


Detail Design Process 5

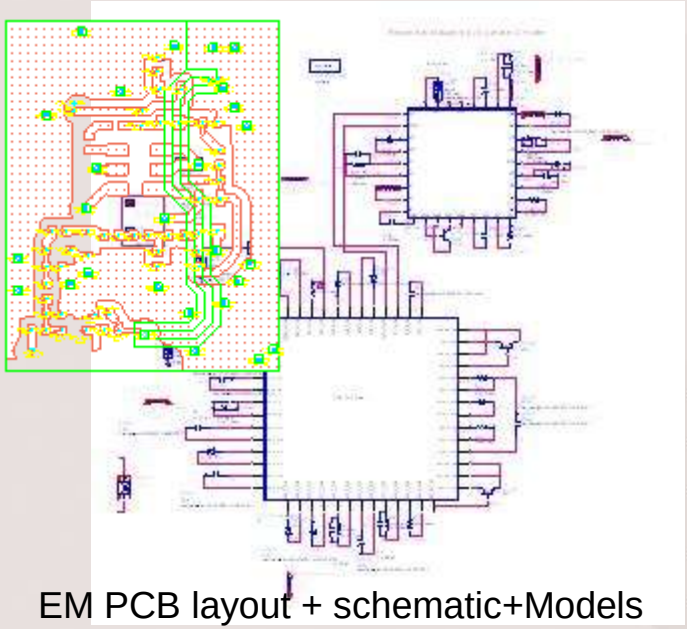


Phase 1 Analysis Report
- RF Test results
- System test results
- Proposed BoM
- Modifications
- Retro-simulations

SCHEMATIC AND EM LAYOUT

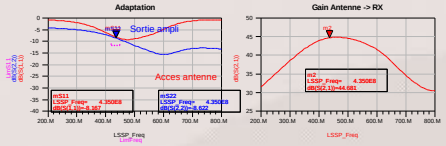


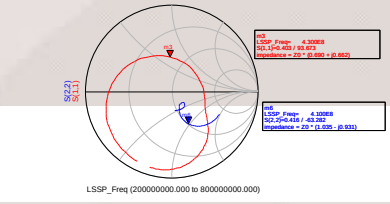
Schematic Only



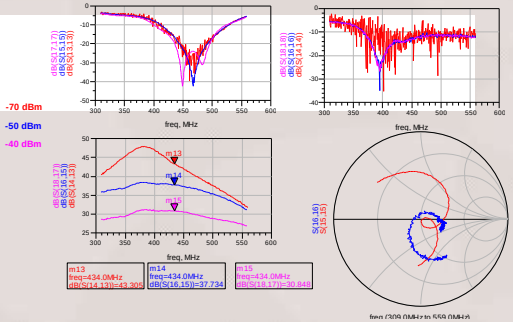
EM PCB layout + schematic+Models

Schematic only Simulation Results

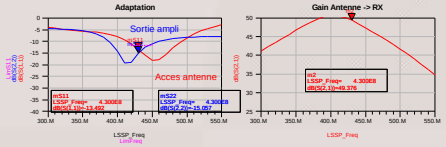


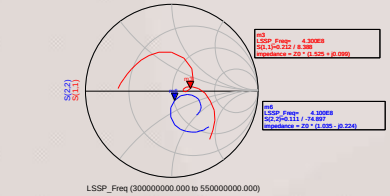


Test Results



EM PCB layout + schematic + models Results

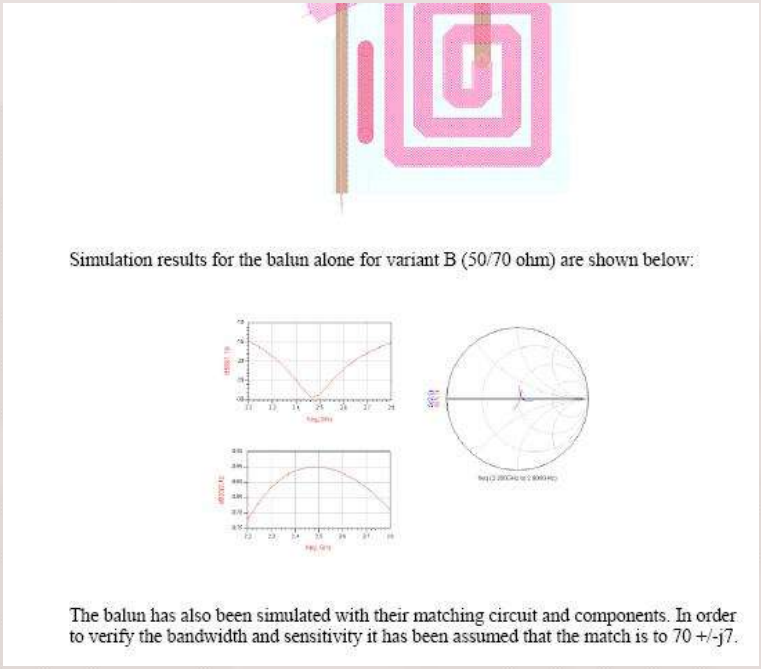


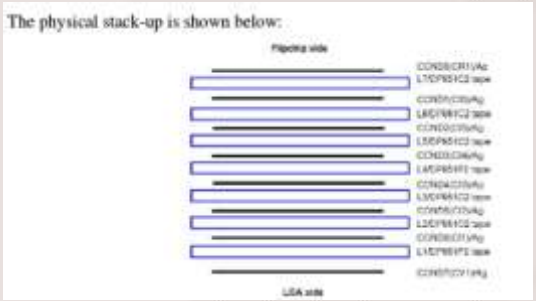


Adjust model complexity for fit

PRELIMINARY DESIGN

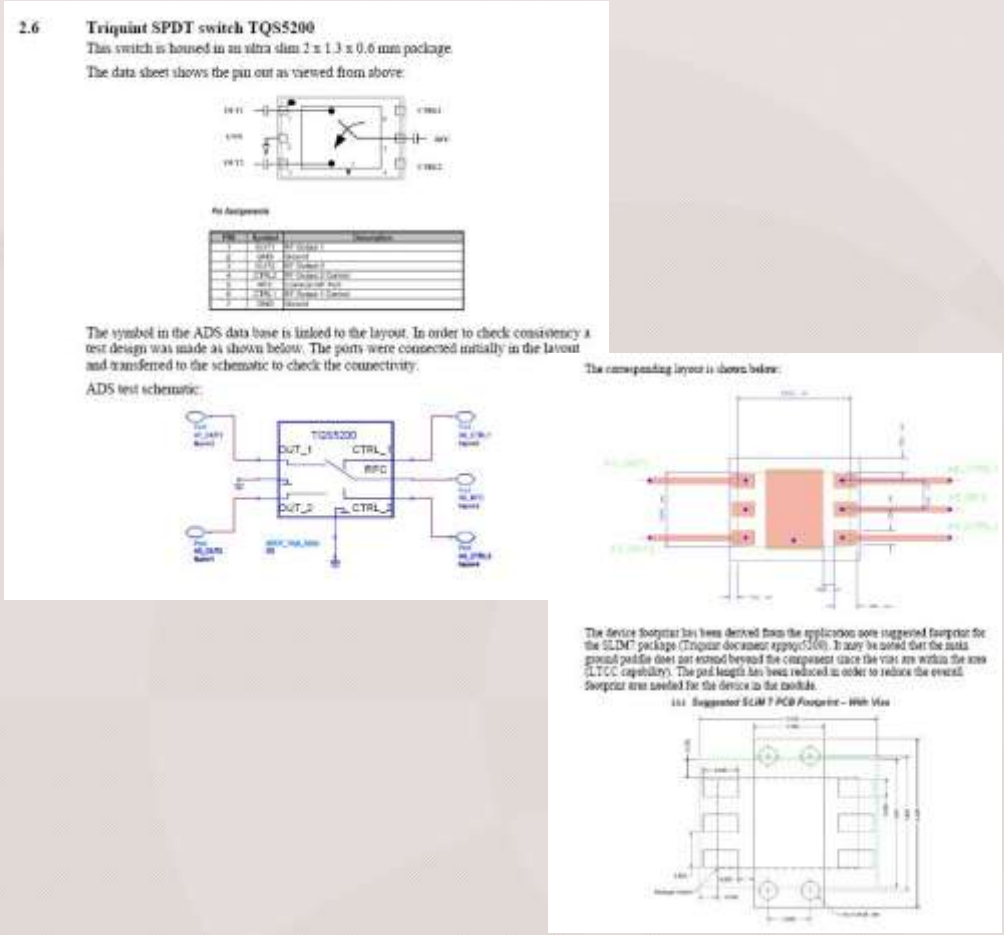
- RF matching
- IPD/SMT split
- Schematic with split
- BoM finalized
- Stack up finalized





DATA BASE VALIDATION

- Compare SMT schematic, pinouts, layout,
  - Supplier data
  - ADS data base
  - Allegro/mentor data base



2.6 **Triquint SPDT switch TQS5200**

This switch is housed in an ultra slim 2 x 1.3 x 0.6 mm package

The data sheet shows the pin out as viewed from above

Pin Assignments

Pin	Symbol	Description
1	OUT1	RF Output 1
2	GND	Ground
3	ANT	RF Antenna
4	CTRL2	DC Control 2 Input
5	RFC	RF Common Port
6	CTRL1	DC Control 1 Input
7	GND	Ground

The symbol in the ADS data base is linked to the layout. In order to check consistency a test design was made as shown below. The ports were connected initially in the layout and transferred to the schematic to check the connectivity.

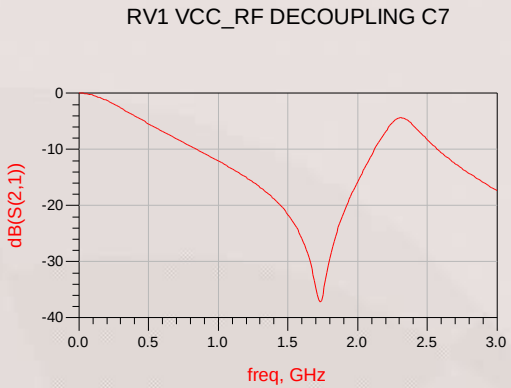
ADS test schematic:

The corresponding layout is shown below:

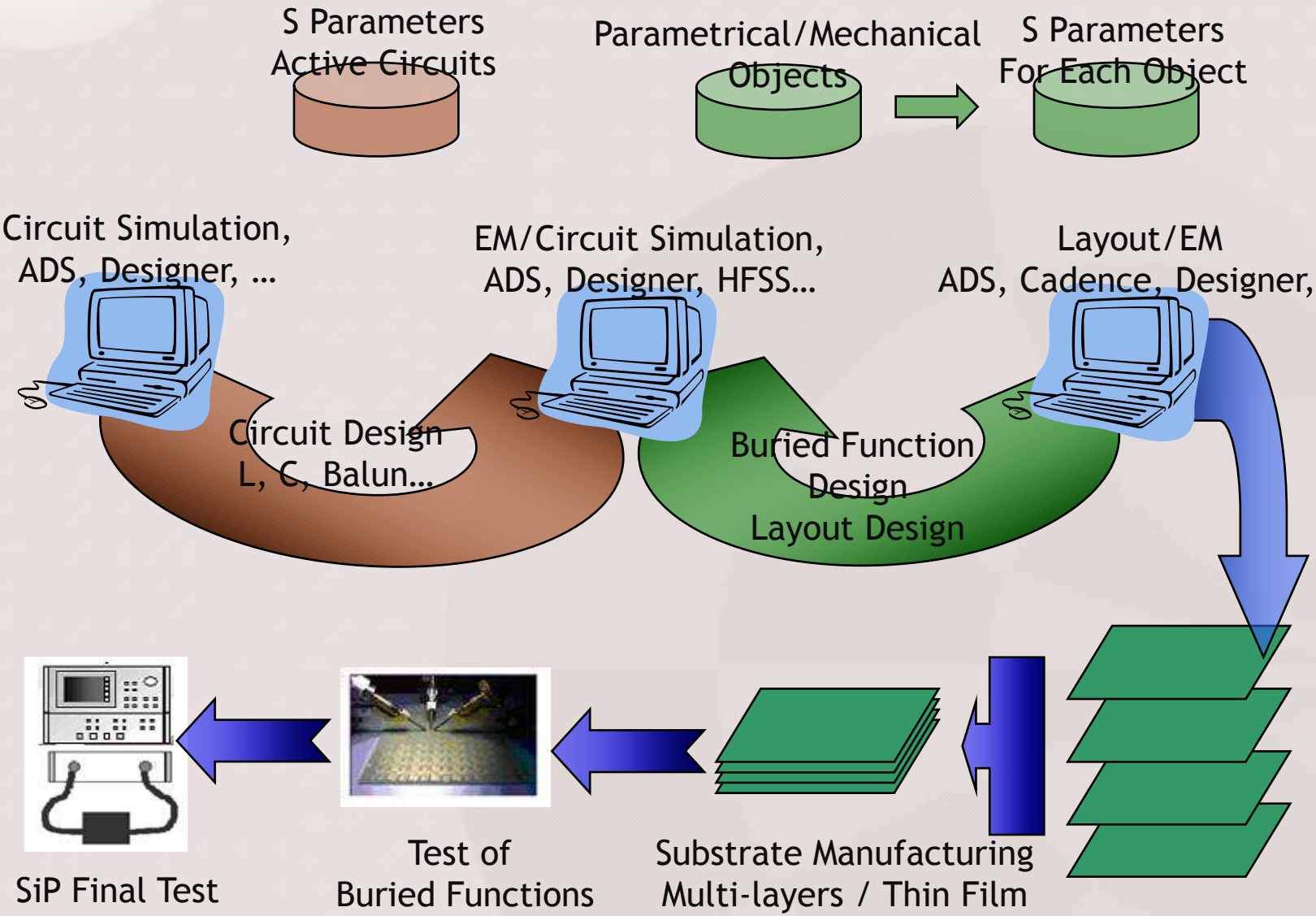
The device footprint has been derived from the application note suggested footprint for the SLIM7 package (Triquint document appnc5200). It may be noted that the main ground paddle does not extend beyond the component since the vias are within the area (LTCC capability). The pad length has been reduced in order to reduce the overall footprint area needed for the device in the module.

DETAIL DESIGN

- RF Design of IPD/LTCC or other
- RF simulation of Laminate/LTCC
- Yield Analysis
- Layout of IPD/LTCC
- Layout of Laminate
- EM Coupling RF to BB and RF to DC
- GDSII and Gerber files
- Design Report

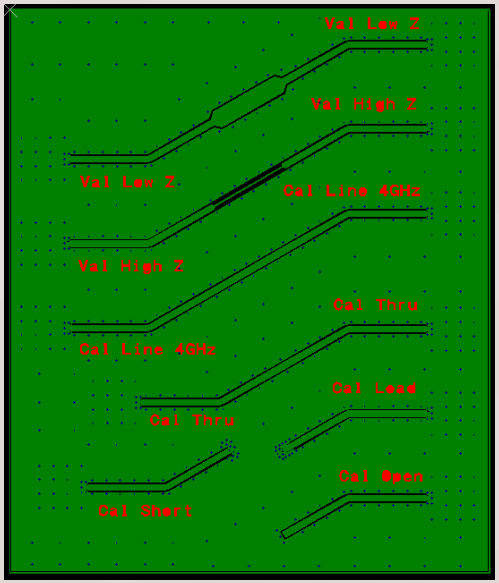


Detail Buried RF Functions



TEST & DEBUG

- System test
  - CMU200 or alternative (Project specific)
- RF testing
  - RS ZVM
  - SMIQ/AMIQ vector signal generators
  - Cascade Probe station
  - Spectrum/modulation Analyser MXA with VSA incorporated for 3G/GSM



Purpose built Cal Kit for VNA

THANK YOU

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