### Simple PCB Design

- **PCB Design - Layout**: 3 weeks
- **PCB Manufacturing**: 1 week
- **Board Assembly**: 1 week
- **Board Debug**: 2-4 weeks

#### Multiple Design Loops

**Board Design**
Typical Lead Time for 1 loop: 7-9 weeks
SiP design
Typical Lead Time for 1 loop: 14-16 weeks
Let’s examine the situation when the design is more complex!!!

➔ More than 2 die, More than 400 connections
COMPLEX PCB DESIGN

More than 5 large LGA, BGA components, More than 500 nets

PCB Design - Layout 3 weeks 4-6 weeks and/or more resources

PCB Manufacturing 1 week 2 weeks

Board Assembly 1 week

Board Test 2-4 weeks 4-6 weeks and/or more resources

Board Design
Typical Lead Time for 1 loop : 11-15 weeks
More than 2 die more than 400 nets Complex RF interactions

SiP Design - Layout
4-8 weeks

EM Simulation
In parallel with SiP design

Substrate Manufacturing
4 weeks

SiP Module Assembly
2-4 weeks

SiP Test
4-6 weeks

One or Two Design Loops

SiP design
Typical Lead Time for 1 loop: 14-22 weeks
OVERALL DESIGN PROCESS

Prepare Contract

Sign Contract

Start phase 1

Design Phase N

Make Protos N

Measure & Analyse Prototypes

Start new phase

OK?

Design Process Complete

Ref Design
Schematic BoM
Proposal, Feasibility Study Report…

Contract
Customer Docs, Specifications,
Schematic Ref Design BoM…

Schematic Layout BoM
Simulation results CDR (DRC OK) for fab

Measurement report
Analysis of results
Determine modifications for next phase
**Preliminary Design**

**Phase 1**

- Sign Contract

- Analyze & Simulate RF part of reference design

- Analyze RF matching From component eval boards

- Confirm Models?
  - **N**
  - Preliminary Matching Design
  - Confirm split IPD/SMT
  - Layout strategy Laminate Stack Up
  - Validate Schematic IPD/Laminate
  - To 2

- **Y**
  - Preliminary Design report:
    - Model validation
    - Basic RF matching
    - Layout strategy description
    - Laminate Stack Up
    - Schematic IPD & Laminate

**Contract**

- Customer Docs
- Schematic Ref Design BoM
- Feasibility Study Report
- Specifications

**DETAIL DESIGN PROCESS 1**
From 1

Create SMT footprints in EDA data-bases

Validate SMT Footprints Cf Data sheets

OK?

N

Y

Detailed IPD layout

Detailed RF Laminate layout

RF Matching & Coupling EM simulation IPD + Laminate

Perf OK?

N

Y

To 3
Design Report:
• RF matching
• EM coupling
• Yield analysis
• IPD CDR
• Laminate CDR
• IPD GDS2
• Laminate Gerber

From 2

Base-band and power supply Layout

EM Coupling BB + RF IPD + Laminate

Perf OK?

N

Y

Monte Carlo Yield Analysis/ Corner Simulations

IPD DRC and CDR

IPD Tapeout

Laminate DRC and CDR

Laminate Tapeout

To 4
From 3

IPD Fab and Bumping

Laminate Fab

Prototype Assembly

Full system Prototype

Power up, DC verification Firmware

System tests End to End

RF by sections + BB

Power up, DC verification Firmware

RF characterization Power, NF, Matching, Gain, Filtering

To 5
From 4

Retro-simulation of RF portion to fit measurements

BoM adjustment and debug

Evaluation Report Modifications for Phase 2

To Phase 2

Phase 1 Analysis Report
- RF Test results
- System test results
- Proposed BoM
- Modifications
- Retro-simulations
Schematic and EM Layout

Schematic Only

EM PCB layout + schematic + models Results

Test Results

Schematic only Simulation Results

Adjust model complexity for fit
RF matching
IPD/SMT split
Schematic with split
BoM finalized
Stack up finalized
• Compare SMT schematic, pinouts, layout,
  - Supplier data
  - ADS data base
  - Allegro/mentor data base
• RF Design of IPD/LTCC or other
• RF simulation of Laminate/LTCC
• Yield Analysis
• Layout of IPD/LTCC
• Layout of Laminate
• EM Coupling RF to BB and RF to DC
• GDSII and Gerber files
• Design Report
DETAIL BURIED RF FUNCTIONS

- Circuit Design
  - L, C, Balun...
- Buried Function Design
- Layout Design
- Substrate Manufacturing
  - Multi-layers / Thin Film
- SiP Final Test
- Test of Buried Functions

- S Parameters
  - Active Circuits
- Parametrical/Mechanical Objects
- S Parameters
  - For Each Object
- Circuit Simulation,
  - ADS, Designer, ...
- EM/Circuit Simulation,
  - ADS, Designer, HFSS...
- Layout/EM
  - ADS, Cadence, Designer, ...
• System test
  - CMU200 or alternative (Project specific)

• RF testing
  - RS ZVM
  - SMIQ/AMIQ vector signal generators
  - Cascade Probe station
  - Spectrum/modulation Analyser MXA with VSA incorporated for 3G/GSM
Thank You

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