BVA (Bond Via Array) Technology for PoP Assembly

Tong Hsing Electronics Industrial Ltd.
Marketing Manager: Po-Hsiu Cheng
Date: 04/22
PHILIPPINE PLANT I

HEADQUARTERS

TAIPEI PLANT

Substrate Fabrication, Hybrids & FT

CP/RW Packaging & Testing

PHILIPPINE PLANT II

LONGTAN PLANT

PHILIPPINES

Substrate Fabrication, Hybrids & CP Testing
<table>
<thead>
<tr>
<th>Tong Hsing Manufacturing Sites</th>
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<tbody>
<tr>
<td><strong>Tong Hsing Manufacturing Sites</strong></td>
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<tr>
<td><strong>Taipei</strong></td>
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<tr>
<td><strong>Address</strong></td>
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<tr>
<td><strong>Established</strong></td>
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<tr>
<td><strong>Employees</strong></td>
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<td><strong>Fax:</strong></td>
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<td><strong>Web Site:</strong></td>
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</table>
Contract Manufacturing for Microelectronic Packaging and Ceramic Thick Film/Thin Film Substrate Fabrication.

- RF Modules
- SiP Packaging
- MEMS Packaging
- Image Sensor Packaging
- Reconstruction Wafer
- Circuit Probing and Final Test
- PCB assembly with SMT and/or COB Processes
- Hybrids Assembly
- Thin Film on Alumina and AlN
- Thick Film on Alumina
- DBC on Alumina and AlN
**RF Examples**

**PA Modules**
- Application: GPS, PCS, CDMA, WiMax, WLAN, LTE
- Frequency: 0.8, 0.9, 1.8, 1.9, 2, 3 GHz
- Package type: LGA
- Substrate: PCB substrate
- Process: SMT + D/B + W/B + Molding + Laser marking + Dicing
- Status: In mass-production

**Front End Modules**
- Application: GPS, PCS, CDMA, WiMax, WLAN, LTE
- Frequency: 0.8, 0.9, 1.8, 1.9, 2, 3 GHz
- Package type: LGA
- Substrate: PCB substrate
- Process: SMT + D/B + W/B + Molding + Laser marking + Dicing
- Status: In mass-production

**MMIC**
- Application: Point-to-point radio application
- Frequency: DC~18G, 10~21G, 20~38G, 34~40G…etc
- Package type: QFN 3X3, 4X4, 5X5, 6X6, 7X7
- Substrate: QFN Leadframe
- Process: D/B + Die Coat (Optional) + W/B + Molding + Plating + Dicing
- Status: In mass-production
SiP Examples

- Application: WiFi + BT
- Frequency: 1.6 & 2.4GHz
- Package type: Single side SiP
- Substrate: PCB substrate
- Process: SMT + Flipchip + Underfill + Metal lid attach + Laser marking + Dicing
- Status: In mass production

- Application: WiFi, GPS, BT, FM, 4 in 1 total solution
- Frequency: 1.6 & 2.4GHz
- Package type: Single side SiP
- Substrate: PCB substrate
- Process: SMT + Flipchip + Underfill + Overmold + Pre-dicing + Sputter + Laser marking + Dicing saw
- Status: In mass-production
Major Strengths

• Flexibility
• Technical Innovation
• Continuous Improvement & Growth
• Excellent High Volume Production Capacity
• Superior Supporting Infrastructure in Northern Taiwan
• Abundant Supply of Human Resources for Semiconductor Packaging in the Philippines
• Superb Customer Satisfaction
• Strong R & D Partners
SiP is the Trend in Mobile Phone

Data from Invensas
Various Package for Small Foot Print

PoP

PiP

STATSchipPAC

fcPiP

15 x 15

543L

Amkor

TMV

14 mm 620 / 230

TMV

Memory Processor

Package PCB

Memory BTo

Process BTo

Package PCB

Except for TSV, the stack packaging infrastructure is well established.

Data from Invensas
Capability of PoP Technologies

Data from Invensas
Basic Concept of BVA Technology

Two molded packages, Top package and Bottom package can be electrically connected together through the vertical wire bonding.
# Capability of PoP Technologies

## BVA PoP: Wide IO Support without TSV

<table>
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</thead>
<tbody>
<tr>
<td><strong>Mobile DRAM</strong></td>
<td>LPDDR</td>
<td>LPDDR2</td>
<td>LPDDR3</td>
<td>LPDDR3 Emerging</td>
<td>Wide IO</td>
<td>Wide IO</td>
<td></td>
</tr>
<tr>
<td><strong>Packaging</strong></td>
<td>PoP</td>
<td>PoP</td>
<td>PoP</td>
<td>PoP</td>
<td>BVA PoP</td>
<td>TSV</td>
<td></td>
</tr>
<tr>
<td><strong>Mobile processor to</strong></td>
<td>168</td>
<td>168</td>
<td>240</td>
<td>240</td>
<td>IO ranging from 200 to 1000+</td>
<td>1200</td>
<td></td>
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<tr>
<td><strong>memory interconnect</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>High IO offers high bandwidth at low speed</td>
<td>200</td>
<td></td>
</tr>
<tr>
<td><strong>Clock Speed (MHz)</strong></td>
<td>400</td>
<td>533</td>
<td>800</td>
<td></td>
<td>Enables intermediate power reductions</td>
<td>0.5X</td>
<td></td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>2X</td>
<td>1X</td>
<td>0.8X</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong># of Channels</strong></td>
<td>Single</td>
<td>Single</td>
<td>Dual</td>
<td>Dual</td>
<td>Quad+</td>
<td>Quad+</td>
<td></td>
</tr>
<tr>
<td><strong>Bandwidth (GB/s)</strong></td>
<td>1.6</td>
<td>4.2</td>
<td>8.5</td>
<td>12.8</td>
<td>≥25.6</td>
<td>≥25.6</td>
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</table>
Vertical Wire Array

- **Vertical Cu Wire Bonding Procedure**
  1. First bond
  2. Wire pre-cut
  3. Pull back & cut off

- **Process Capability**
  - Wire Material: Cu plated Pd / Cu plated Pd,Au
  - Wire Diameter: 1mil / 1.5mil / 2mil
  - Minimum Loop Height: 290um
  - Maximum Loop Height: 800um
  - Minimum Pad Pitch: 240um
Vertical Wire Bonding

- The nominal height of the wire-bonds is 0.5 mm.

Data from Invensas
Molding

Bottom Cavity goes up…

Stops at the soft clamp and slowly closes (parameter setting)…

Molding…

Bottom Cavity goes back down…
Molding and Tip Exposure

- Exposed Vertical Wire
## BVA Reliability

<table>
<thead>
<tr>
<th>Test</th>
<th>Standard</th>
<th>Test condition</th>
<th>Sample size</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Moisture sensitivity Level 3</td>
<td>IPC/JEDEC-J-STD-020C</td>
<td>125°C for 24hrs; 30°C/60%RH for 192 hrs, 3X Pb-free reflow</td>
<td>22 logic and 22 memory packages</td>
<td>Pass</td>
</tr>
<tr>
<td>High temperature storage</td>
<td>JESD22-A103D-condition B</td>
<td>150°C, 1000 hours</td>
<td>22 PoP off-board</td>
<td>Pass</td>
</tr>
<tr>
<td>Unbiased autoclave</td>
<td>JESD22-A102D-condition D</td>
<td>121°C/100%RH/2atm for 168 hours</td>
<td>22 PoP off-board</td>
<td>Pass</td>
</tr>
<tr>
<td>Drop test</td>
<td>JESD22-B111</td>
<td>&gt;30 drops, 1500 G, 0.5 msec of half sine pulse</td>
<td>20 PoP on board with underfill</td>
<td>Pass (no failures till 128 drops)</td>
</tr>
<tr>
<td>Temperature cycling (board level)</td>
<td>JESD22-A104D Condition G</td>
<td>-40°C to 125°C, 1000 cycles</td>
<td>45 PoP on board with underfill</td>
<td>Pass</td>
</tr>
</tbody>
</table>

- BVA PoP successfully passed all standard reliability tests.
BVA on Memory & MCU

- Stand-off issue eliminated: Wire-bond based memory-logic interconnect
- 1000+ wide IO: 0.2 mm pitch easily possible
- High performance at low-cost: Conventional PoP materials and processes
The logic substrate has flip chip in the center, and wire-bond pads along the periphery.

The memory substrate has solder pads along the periphery.

Conventional industry equipment and processes are used to assemble the BVA PoP.
BVA SiP Advantages

BVA is 3D Vertical Interconnect Technology suitable for MEMS, RF etc System-in-Package (SiP) applications

- Smaller Footprint: Vertical integration with existing wire bond process
- Lower Cost: Fits many active Si and passives in small footprint
- Reliable Performance: Reliable for long life applications
- Flexible Supply Chain: Easily scalable supply chain

Company Confidential
Example BVA SiP for RF Module

- Additional plane for SMT without interposer
- Reduced parasitic between die to passives
- Shorter interconnect between die
- 40% reduction in SiP component footprint

40% area reduction
Example BVA for Image Sensor
Summary

• BVA technology is invented and developed by Invensas. This novel technology can offer higher I/O and high aspect ratio interconnection for PoP module.

• The vertical wire technology has been applied to Fan-out process for interconnection in Tong Hsing. We used it for several image sensor package development.

• In additional to the OEM service, Tong Hsing develop suitable package method and work with customer to verify the advanced package approach for future requirement.