



*Insight SiP*

# Insight SiP



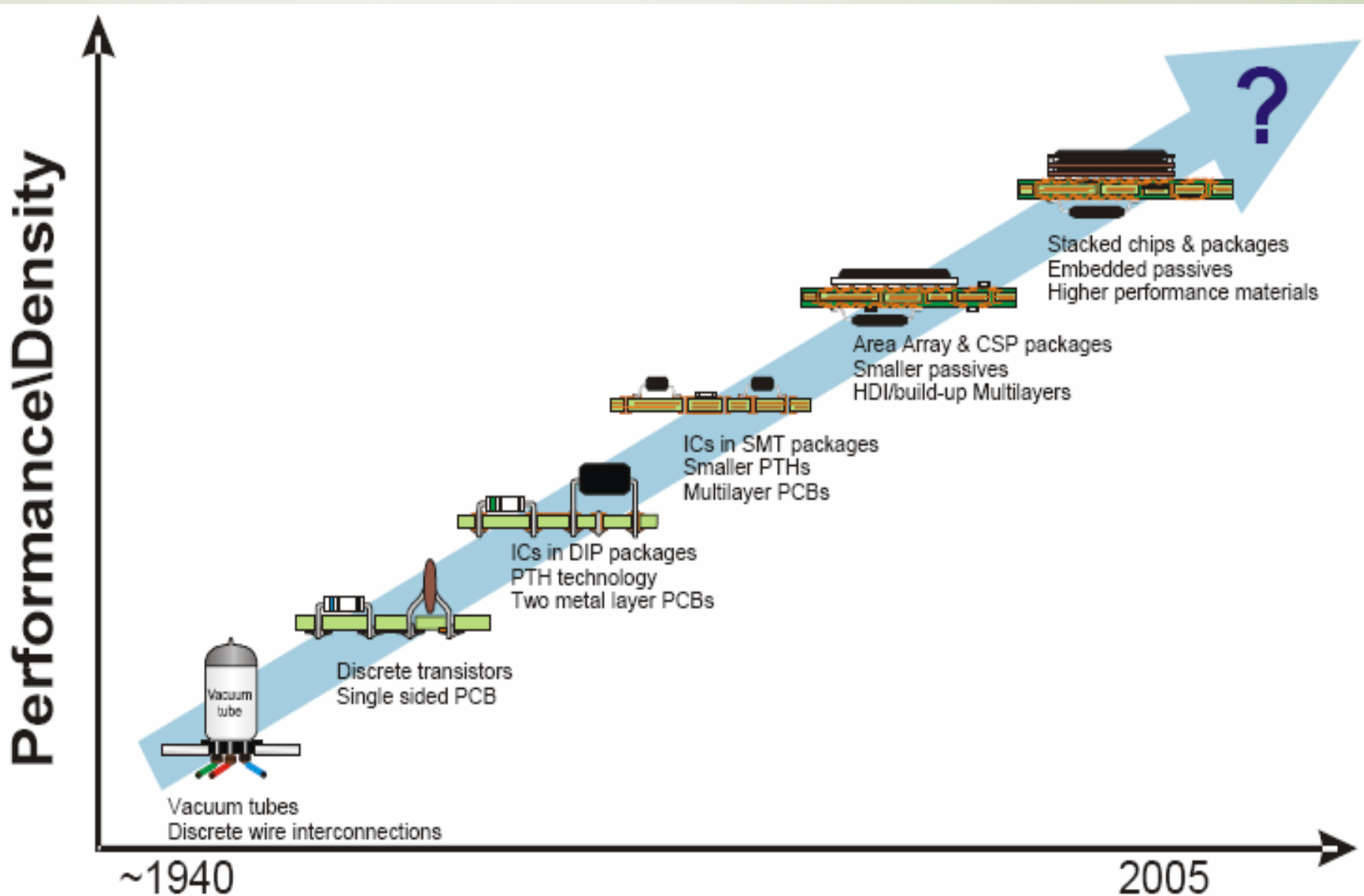
# Company



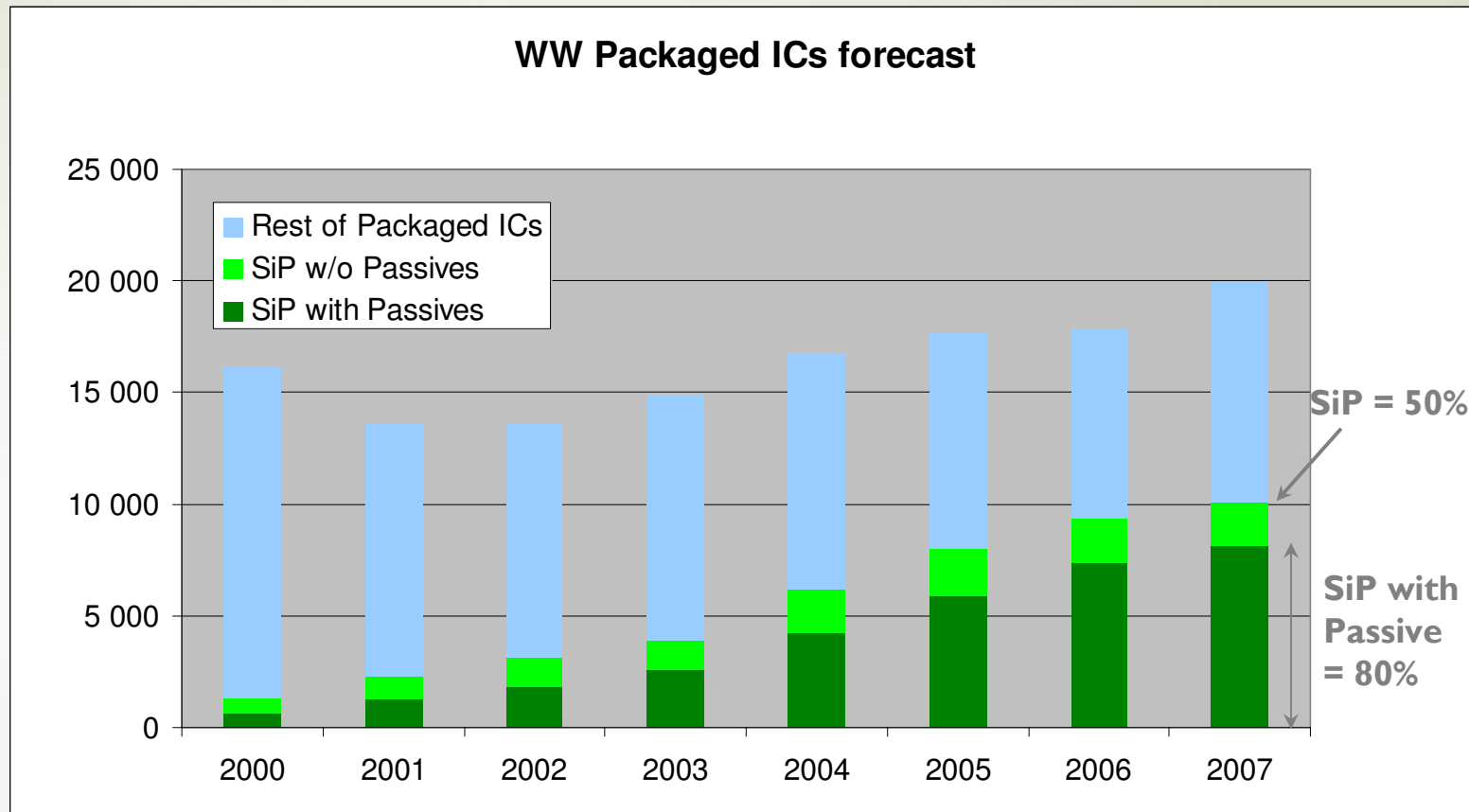
- Insight SiP founded in 2005 in Cambridge UK
- French Headquartered Company, Sophia-Antipolis
- Core Team from Alcatel, Lucent Technologies, Motorola, NSC, Thales, Murata, Philips and TI
- 10 senior RF designers
- Office in the US in Q4, 2007



# Moore's law in Electronics

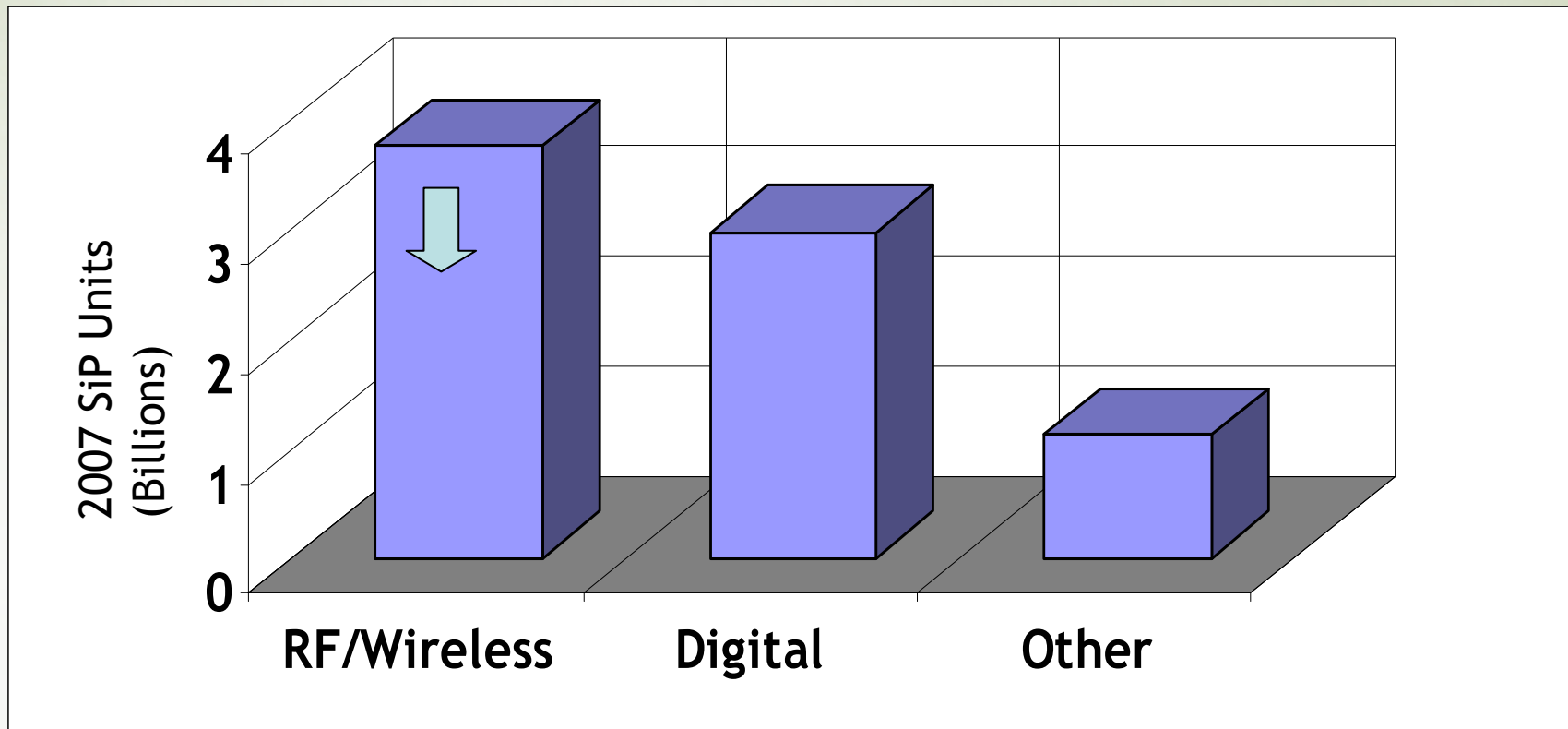


# Market SiP figures



Source: Gartner, March 2005

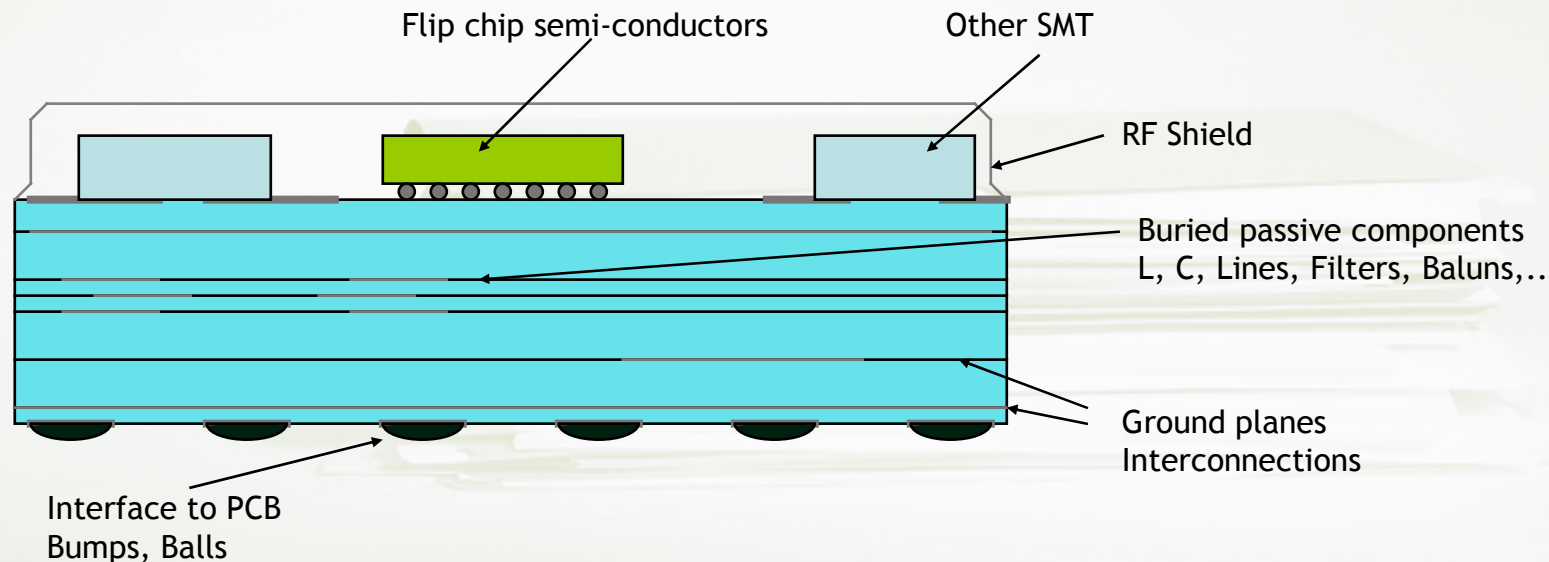
# Market Target



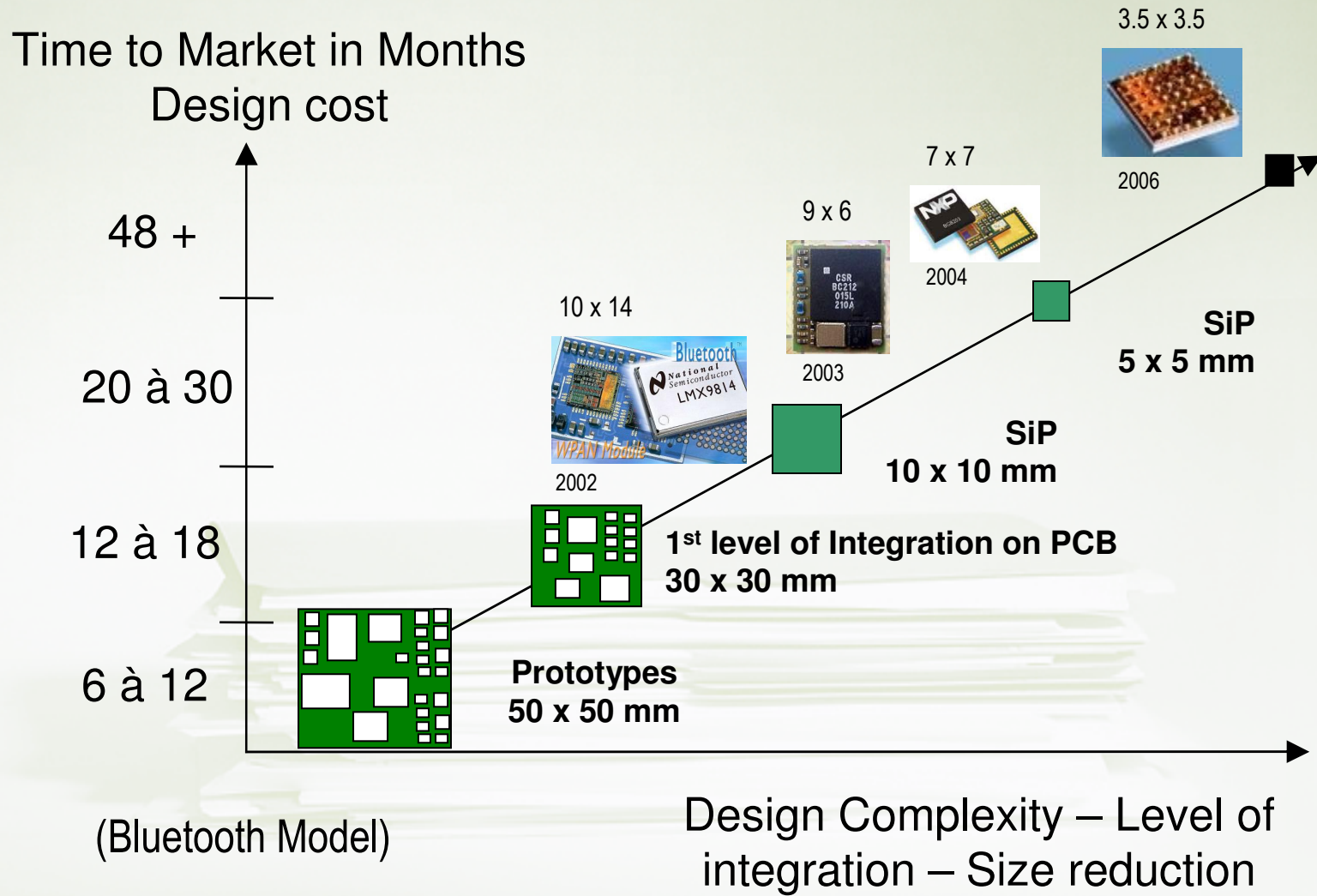
Sources: Prismark (primary), Deutch Bank, Credit Suisse First Boston, Allied Business Intelligence.

# System-in-Package

- “RF System in a Package”
  - Complete 3D RF system designed including
    - RF semi-conductors
    - Base-band semi-conductors
    - SMT passives
    - Buried RF passives
    - Interface to application PCB (LGA, BGA)



# SiP life cycle





# SiP vs SoC

Parameter	SiP	SoC
Development Costs	x 1 Millions \$	x 10 Millions \$
Development Duration	12 to 15 months	more than 3 years
Time to market	1 yr	3 - 4 yrs
Technology mix	Yes Filters/Xtal	No
Typical size	5 x 5 x 1.4 mm	3 x 3 x 0.9 mm
Need for external components	No	Yes
Production costs	Low	Very low



## Insight SiP technical offer

- Design and manufacturing of highly integrated custom (RF) systems and sub-systems :
  - Based on System in a Package (SiP) approach
  - RF/Analogue **focused design**
  - **Multi-technologies** : PCB, LTCC, Thin film, Thick film...
  - Emphasis on optimum **overall cost** in production
  - Matching the design to **current world-wide manufacturing capability**
    - → Optimizing the technology choices for **size, cost and time to market**



## Insight SiP technical offer

- **Insight SiP** has access to world leaders design rules for each SiP manufacturing technology.
  - Amkor - Korea - Micro packaging
  - ASE - Taiwan - Micro packaging
  - AT&S - Germany - Laminate Substrates
  - D.T.M - Taiwan - LTCC Substrates
  - Kyocera - Japan - LTCC Substrates
  - NXP - France - SbSiP Substrates
  - Tong Hsing Electronics - Taiwan - Micro packaging
  - Unisem - UK & Asia - Micro packaging

# Success Stories

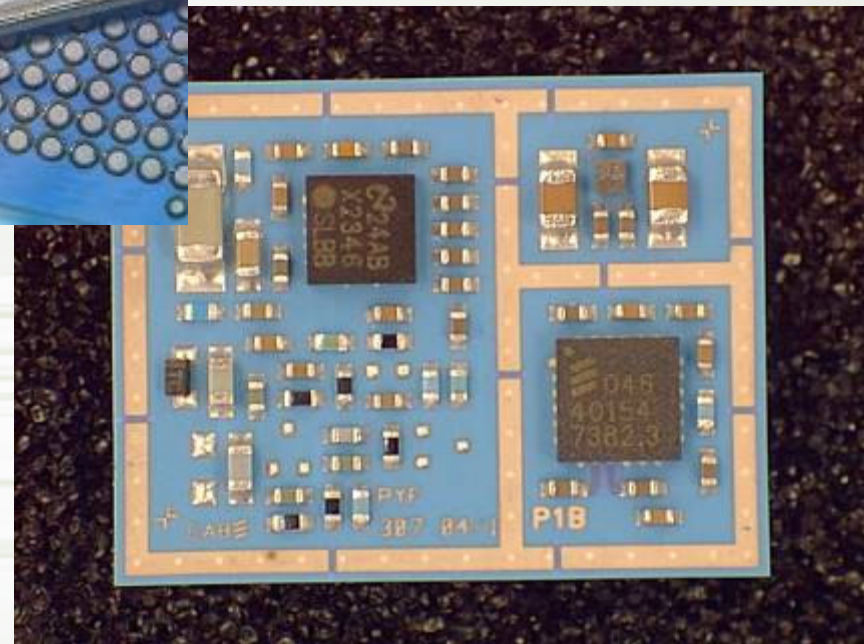


## Bluetooth Module LMX9814 for NSC

- from design to volume manufacturing

## RF Function for Ericsson

- from co-design to production



# Success Stories



## Wifi Module NRG723 for Nanoradio

- from design to volume manufacturing

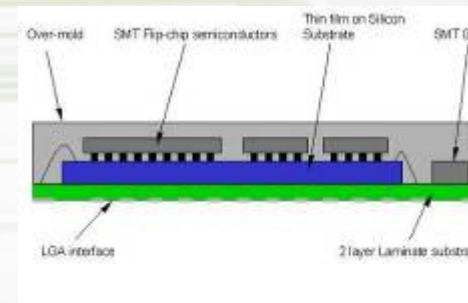
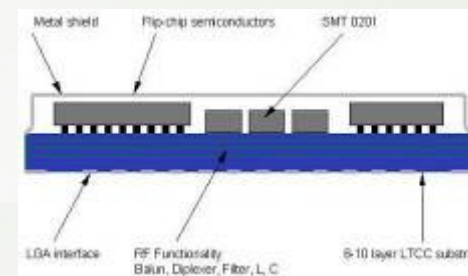
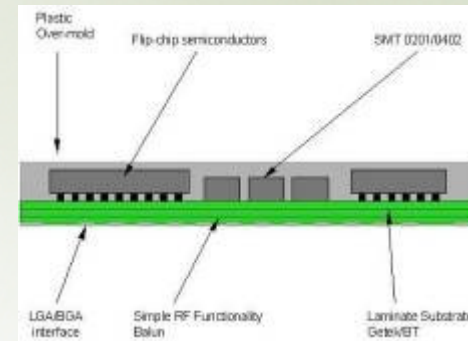
## ISM IQ Mixer for Atlantic RF

- from design to production



# SiP Technologies

- Laminate based ( $\epsilon_r$  3 - 5)
  - 4 to 6 metal layers
  - Interco. RF Baluns in substrate
- LTCC based ( $\epsilon_r$  7 - 10)
  - 6 to 20 metal layers
  - Interco. RF baluns, Filters, matching in substrate
- Silicon Based ( $\epsilon_r$  11.2)
  - 2 to 4 metal layers + doping
  - Interco. RF baluns, Filters, matching and high C in substrate



# Insight's PRD Design

- Step 1 : Feasibility Study and Specifications
- Objective : choose the Best Architecture to Optimise
  - Performances according to the Market Requirement,
  - Production and Development Costs,
  - Design to Production Lead Time.
- Method :
  - System partition
  - Semiconductors Technology Choice : Si, GaAs, SiGe,...
  - SiP Technology Choice : Laminate, LTCC, SbSiP
  - Assembly options (Flip-chip vs Bond-wires)
  - Buried passives vs Si passives vs SMT
  - Compare SiP substrates
    - Size
    - Cost
    - NRE
- Typical Timing : 4 to 10 weeks
- Deliverable : Feasibility Study Report

# Insight's PRD Design - Step 1

## UWB LTCC Module

Description	Part #	Die size	Package dimensions		Component area	Courtyard Dimensions IPC7351		Courtyard area	Max Height	Quantity	Total courtyard area	Total Component area
			X	Y		X	Y					
<i>Dimensions</i>		mm x mm	mm	mm	mm <sup>2</sup>	mm	mm	mm <sup>2</sup>	mm		mm <sup>2</sup>	mm <sup>2</sup>
<b>Actives</b>												
RF + BB SoC	UWB_XX_100 Flip chip	5 x 5	5	5	25	5,5	5,5	30,25	0,5	1	30,25	25
Total Actives											30,25	25
<b>RF Passive Functions</b>												
3 to 5 GHz UWB Filter	Buried in LTCC					5	4	20	0	1	20	0
Total RF passive functions in LTCC buried layers											20	0
<b>RF C, L buried in LTCC</b>												
Capacitors	<22pF					1,5	1,5	2,25	0	5	11,25	
Inductors	<27nH					1,2	1,2	1,44	0	5	7,2	
Total RF C,L buried in LTCC											18,45	
<b>Total use of internal LTCC layers</b>											<b>38,45</b>	
Crystal	NX2520SA 40MHz	2520	2	2,5	5	3	3,5	10,5	0,65	1	10,5	5
Total Crystals											10,5	5
<b>Passives</b>												
	0201 Capacitors Decou	CD201	0,5	0,3	0,15	1,1	0,5	0,55	0,4	10	5,5	1,5
	0402 Capacitors Decou	CO402	1	0,5	0,5	1,5	0,75	1,125	0,6	3	3,375	1,5
	0201 Inductors	LD201	0,5	0,3	0,15	1,1	0,5	0,55	0,4	0	0	0
	0201 Resistors	RO201	0,5	0,3	0,15	1,1	0,5	0,55	0,4	1	0,55	0,15
Total Passives											9,425	3,15
<b>Maximum Height of components</b>									<b>0,65</b>			
<b>Total sum of courtyards</b>											<b>50,175</b>	<b>33,15</b>
<b>Estimated dimensions with 0.2mm keput for overmold</b>											<b>7</b>	<b>8</b>

## Overall Estimated Size

**7      8      1,4**

Item	Height estimation
	mm
Substrate	0,5

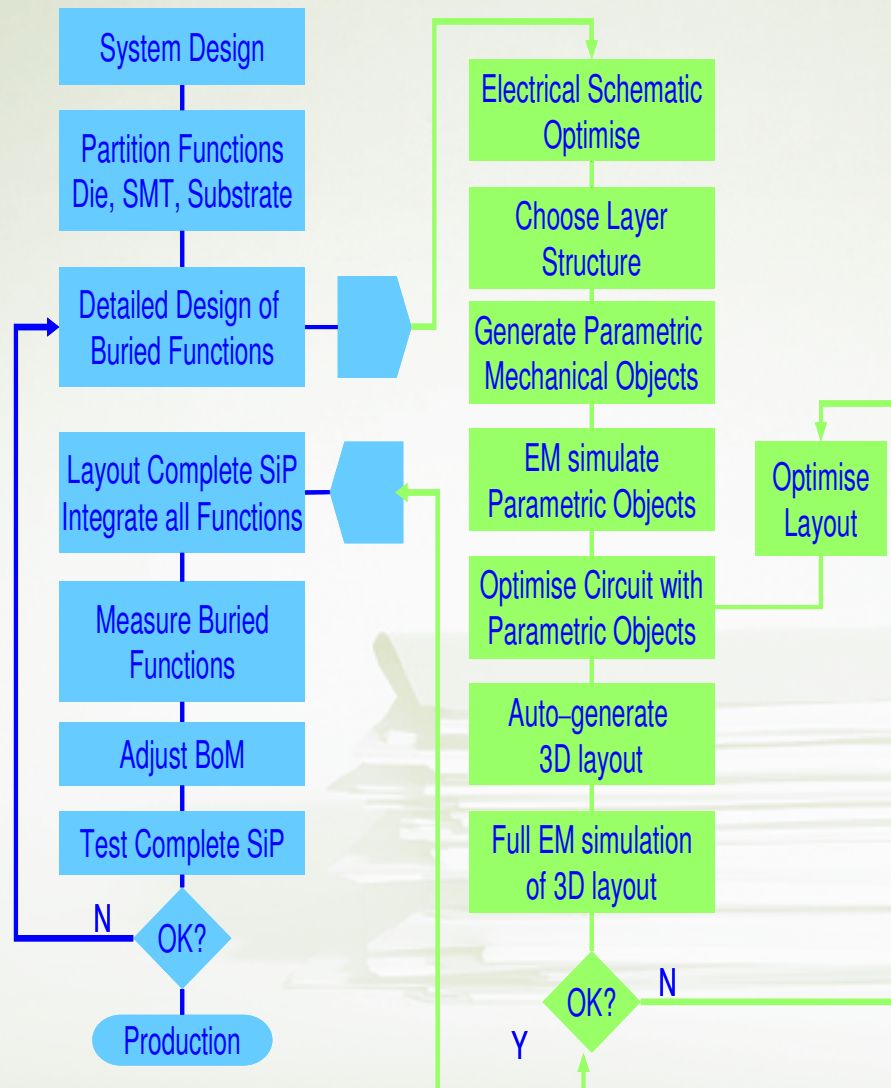
# Insight's PRD Design - Step 1

UWB Laminate Module				UWB SbsiP Module																			
Description	Part #	Die size mm x mm	Package dimensions X Y mm mm	Component area	Court yard Dimensions IPC7351		Court yard area	Max Height	Quantity	Total court yard area	Total Component area												
					X	Y																	
Dimensions		mm x mm	X Y	mm																			
Actives																							
RF + BB SoC	UWB_XX_100 Flip chip	5 x 5	5 5																				
Total Actives																							
RF Passive Functions																							
3 to 5 GHz UWB Filter	Filter on top LTCC	3 x 4	2 4																				
Total RF passive functions																							
RF C, L																							
Capacitors	+22pF	0,5	0,3																				
Inductors	+27nH	0,5	0,3																				
Total RF C,L																							
Crystal	NK2520SA 40MHz	2520	2 2,5																				
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Passives	0201 Capacitors Decou C0201	0,5	0,3																				
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	0201 Inductors L0201	0,5	0,3																				
	0201 Resistors R0201	0,5	0,3																				
Total Passives																							
Maximum Height of components																							
Total sum of court yards																							
Estimated dimensions with 0.2mm keupot for overmold																							
<b>Overall Estimated Size</b>																							
	<b>8</b>	<b>10</b>	<b>1,4</b>																				

UWB LTCC Module												Height estimation			
Description	Part #	Die size mm x mm	Package dimensions X Y mm mm	Component area	Court yard Dimensions IPC7351		Court yard area	Max Height	Quantity	Total court yard area	Total Component area				
					X	Y						mm <sup>2</sup>	mm <sup>2</sup>	mm	mm <sup>2</sup>
Dimensions		mm x mm	X Y	mm <sup>2</sup>	X	Y	mm <sup>2</sup>	mm			mm <sup>2</sup>	mm <sup>2</sup>			
Actives															
RF + BB SoC	UWB_XX_100 Flip chip	5 x 5	5 5	25	5,5	5,5	30,25	0,5	1	30,25	25				
Total Actives															
RF Passive Functions															
3 to 5 GHz UWB Filter	Buried in LTCC				5	4	20	0	1	20	0				
Total RF passive functions in LTCC buried layers														20	0
RF C, L buried in LTCC															
Capacitors	<22pF				1,5	1,5	2,25	0	5	11,25					
Inductors	<27nH				1,2	1,2	1,44	0	5	7,2					
Total RF C,L buried in LTCC														18,45	
Total use of internal LTCC layers														<b>38,45</b>	
Crystal	NK2520SA 40MHz	2520	2 2,5	5	3	3,5	10,5	0,65	1	10,5	5				
Total Crystals														10,5	5
Passives	0201 Capacitors Decou C0201	0,5	0,3	0,15	1,1	0,5	0,55	0,4	10	5,5	1,5				
	0402 Capacitors Decou C0402	1	0,5	0,5	1,5	0,75	1,125	0,6	3	3,375	1,5				
	0201 Inductors L0201	0,5	0,3	0,15	1,1	0,5	0,55	0,4	0	0					
	0201 Resistors R0201	0,5	0,3	0,15	1,1	0,5	0,55	0,4	1	0,55	0,15				
Total Passives														9,425	3,15
Maximum Height of components														0,65	
Total sum of court yards														50,175	33,15
Estimated dimensions with 0.2mm keupot for overmold														7	8
<b>Overall Estimated Size</b>															
	<b>7</b>	<b>8</b>	<b>1,4</b>												
Item												Height estimation			
Substrate												mm	0,5		

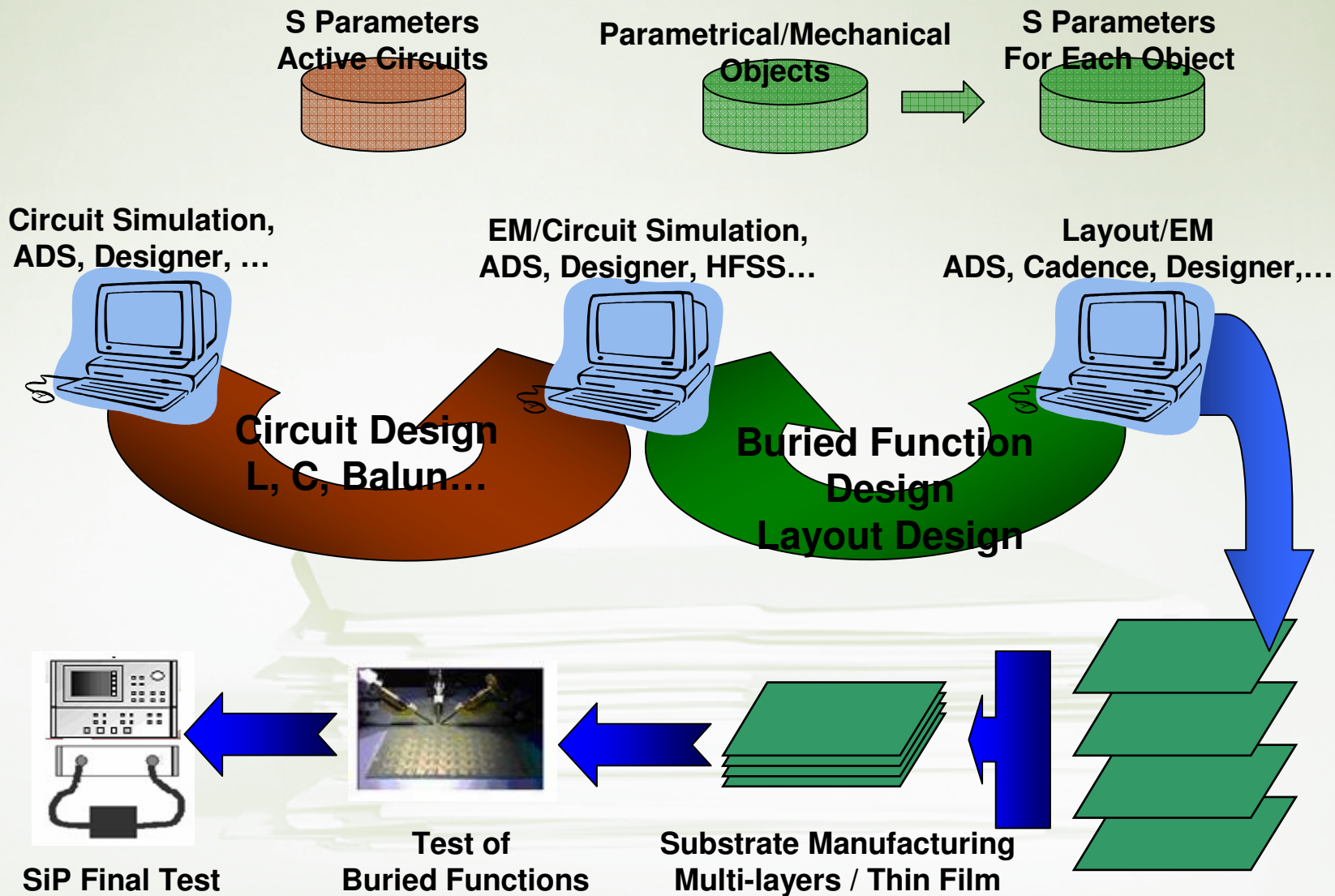
- SiP Technology Comparison
  - Size & Performances
  - Cost & Time to Production

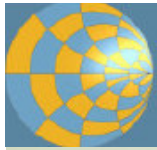
# Insight's PRD Design - Step 2



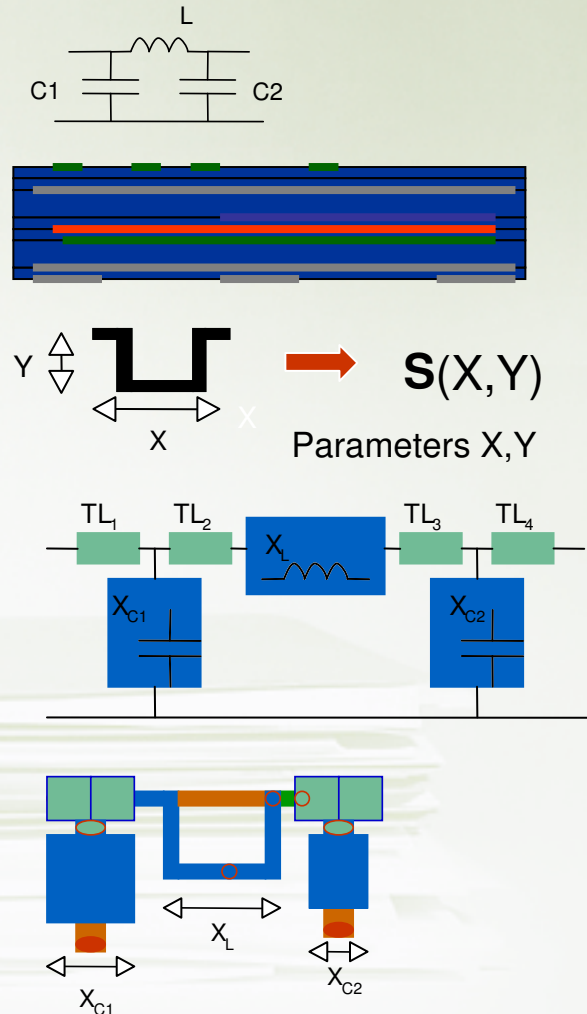
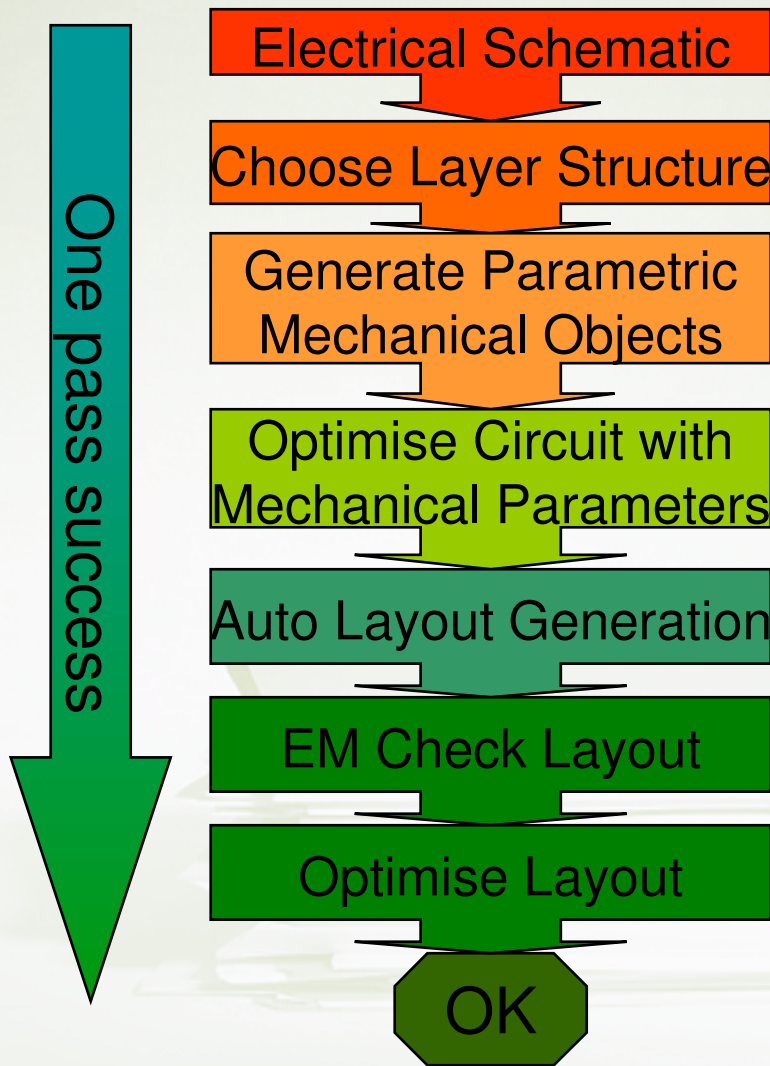
- Standard EDA software based.
- Step-by-step Process
  - System model development
  - Project-specific component library
  - Circuit Optimization taking interactions into account
  - Exhaustive simulation of electro-magnetic behavior
  - Performance Optimization through electro-magnetic simulation feedback to circuit model.
  - Proven two-pass success (with one-pass objective)

# Insight PRD Design - Step 2





# Design flow for buried functions

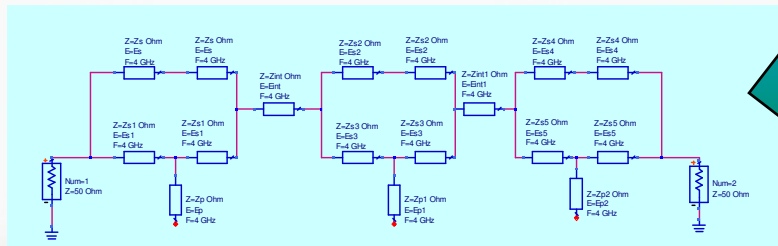


# UWB filter example

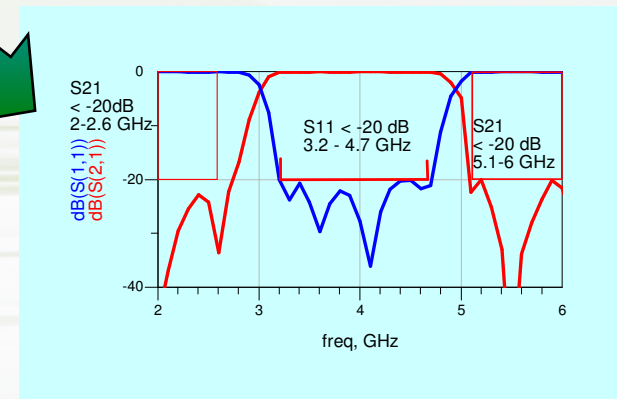
- Specification

Parameter	Units	Spec	Comments
IL	dB	< 4	3.2 to 4.7 GHz
RL	dB	>20	3.2 to 4.7 GHz
Rej WLAN b/j	dB	>20	2 to 2.6 GHz
Rej WLAN a	dB	>20	5.1 to 6 GHz

- Initial Circuit Idea

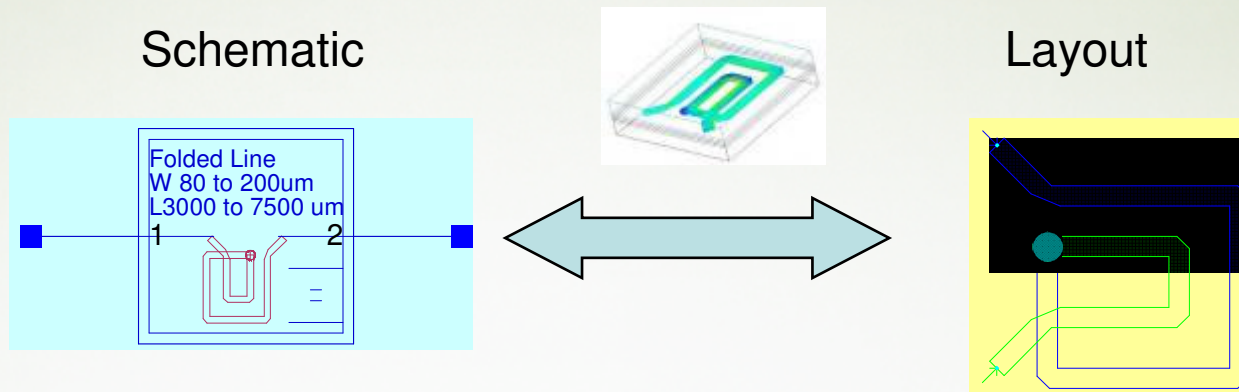


- Optimised Filter Response

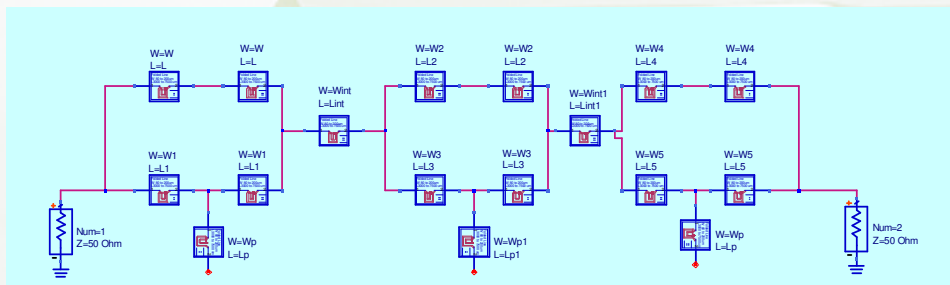


# UWB filter example

- Generate Parametric Objects using EM simulator



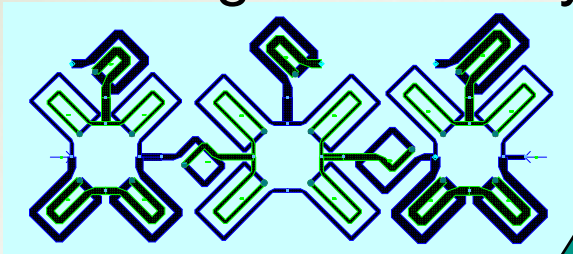
- Optimize Circuit with Parametric Objects



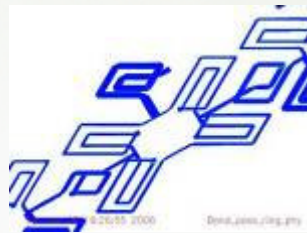


# UWB filter example

- Auto-generate Layout



- Simulate layout



- Optimise to lock performance

