RF System in Package Design for Portability between suppliers and technology platforms

Abstract

Today, the System-in-Package approach offers a new dimension to system integration, far beyond mere dense micro-packaging of existing System on Chip solutions. Not only does SiP offer the capability to integrate almost any kind of companion passive component with a given active circuit, but it also enables flexible combinations of analogue circuits and RF functions with digital integrated circuits. The SiP approach is a key driver for the miniaturization trend for portable devices (Cell-phones, PDAs, Ultra-miniature PCs), particularly with respect to the growing number of RF functions that need to be integrated.

Most SiP design methodologies, that include integrated passive components, rely on fixed libraries of components that are locked to a particular substrate supplier and stack-up. For high volume consumer devices it is increasingly important to ensure that any given SiP can be sourced from at least two independent manufacturers.

The novel design methodology that is presented in this paper is aimed at allowing easy transfer of integrated passive circuit design from one supplier to another and even from one technology to another (e.g. LTCC to IPD).

The methodology is based on a user extendable library of mechanical objects for which the electrical models are created automatically for a given stack-up and/or technology. Thus any design that is initially made for a particular supplier can easily be re-tuned for an alternative source.

The second manufacturer can have a completely separate set of electro-mechanical parameters (stack-up, dielectric constant, layer thickness, loss factors, metal types) and may even use an alternative technology.

The paper will illustrate the design method with some examples of RF SiP designs that have been ported between LTCC suppliers and between LTCC and IPD technologies.

Introduction

The SiP approach to RF system integration has become essential to the miniaturization road-map for nomadic devices. Despite a long term tendency to integrate more and more functions within a single semiconductor (SoC approach) the never ending increase in functionality for small personal devices continues to drive the use of SiP to make complete systems.

RF SiP can be realized using a multitude of technologies; for each technology a range of suppliers offer different materials, physical dispositions and properties, that require any design to be matched to the particular supplier. In this paper the following technologies are considered:
Organic multi-layer laminate with small SMTs, Ceramic multi-layer substrates (LTCC), Integrated Passive Devices (using thin film on silicon or glass), a combination of the above.

An example of an RF SiP is shown in Figure 1.

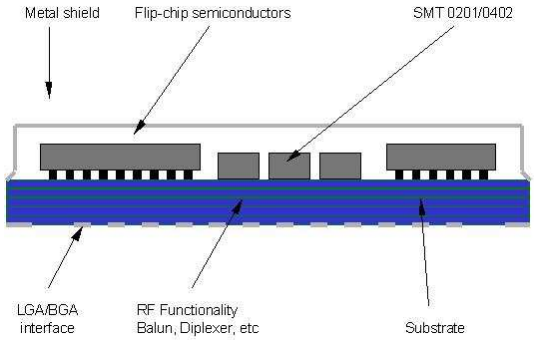

Figure 1 RF SiP

High volume RF SiP should be at least double sourced. In order to use 2 different supply chains the design must be adjusted to take into account the differences between the suppliers. In certain situations it may be necessary to use 2 different supply chains using different SiP technology mixes.

This paper describes a universal RF SiP design methodology that is sufficiently flexible to allow for a design to be transferred rapidly between different technologies or between suppliers using the same technology.

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Design Methodology

The design methodology developed at Insight SiP has already been described in previous communications[1,2]. The methodology is summarized in Figure 2.

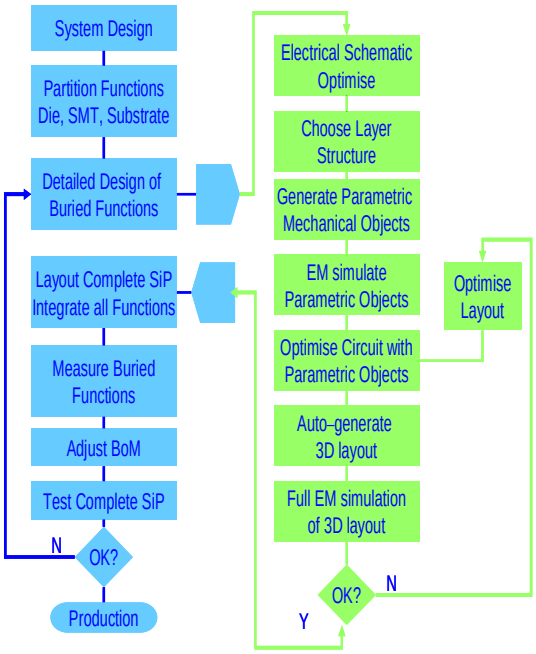

Figure 2 Insight SiP Design Methodology

The method uses a combination of circuit and electromagnetic simulation tools to create a design progressively from basic schematic representation to a complete 3D electromagnetic representation of the layout. Manufacture is only carried out on a design for which the completed layout has been fully simulated; 2.5D or 3D electromagnetic simulations are used for the passive integration (laminate, LTCC, IPD) and harmonic balance or Spice modelling for the active circuits.

The complete design flow from initial schematic based circuit simulation to fully simulated and tested layout is shown in Figure 3.

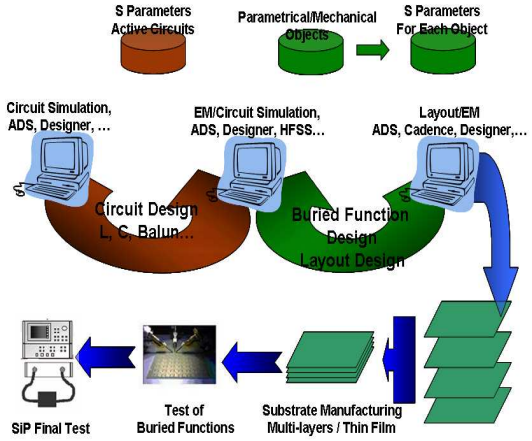

Figure 3 Design Flow Schematic to tested Layout

Technology File Definitions

RF SiP uses a combination of Organic Laminate substrates, Ceramic LTCC substrates and Thin Film Silicon or Glass IPDs.

Each technology and each supplier may be characterized by a technology file that describes the material parameters and physical disposition between the dielectric and metallic layers. In the case of organic and ceramic laminates each supplier has a range of materials and layer structures that may be used.

Figures 4 to 6 show typical technology files for LTCC, IPD and Laminate options.

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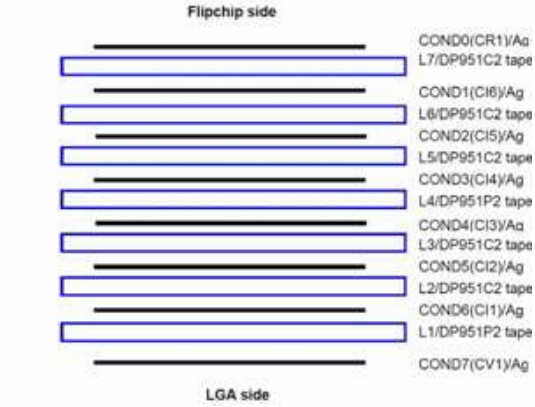
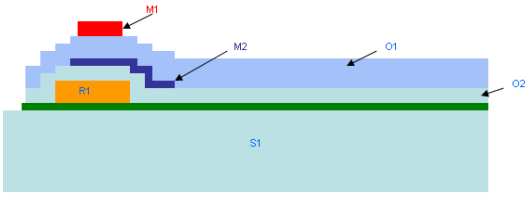


Ceramic Tape
Dupont 951
εr : 7.8
Tanδ : 0.005
C2 thickness 40µm ± 5 µm
P2 thickness 125 µm ±10 µm
Thick Film Silver CV1, CR1, CI1 to CI6
Thickness 10 µm ±3 µm
Conductivity 4.5 x 10^{7}

Figure 4 Typical LTCC Technology File



M1 – Metal layer 1
Thickness 5 µm ± 0.5 µm
σ = 5 x 10^{7} S/m
O1 – Oxide layer 1
Thickness 0.6 µm ± 0.05 µm
ε_r 4.0
M2 – Metal layer 2
Thickness 2 µm ± 0.4 µm
σ = 3 x 10^{7} S/m
O2 – Oxide layer 2
Thickness 0.5 µm ± 0.1 µm
εr 4.5
R1 – Resistor layer
10 ohm/squ ± 1 ohm/squ
S1 – Substrate HR Si 2 kohm.cm
Thickness 250 µm ± 20 µm
εr 12
σ = 0.05 S/m

Figure 5 Typical IPD Technology File

Layer	Material Type	Nominal Thickness (um)
Solder Mask		20
Outer Copper	Plated Copper	20
Prepreg_1	Prepreg	40
Inner Copper	Plated copper	20
Core laminate	CCL	60
Inner Copper	Plated copper	20
Prepreg_2	Prepreg	40
Outer Copper	Plated Copper	20
Solder Mask		20
Total Thickness		260

BT Dielectric properties
ε_r 4.7
Tanδ 0.013
Copper Conductivity 5 x 10^{7} S/m

Figure 6 Typical Laminate Technology File

In order to fully characterize each technology for simulation purposes it is essential to have a minimum set of data. This should include dielectric material properties for all layers (εr, tanδ at operating frequency), conductivity for all metallic and resistive layers plus the mechanical dimensions.

In addition to the basic nominal parameters, the manufacturing tolerances allow yield predictions and worst case corner analyses to be carried out.

Mechanical Objects

The methodology described above allows any of the above technologies to be designed using the same basic flow. The functionality that is contained within buried functions inside the substrate is created using an iterative process. For each technology a range of parameterized mechanical objects has been created. These objects allow simple RF functions, such as capacitors, inductors and resonators, to be created.

A couple of typical mechanical objects are shown in Figure 7 and Figure 8.

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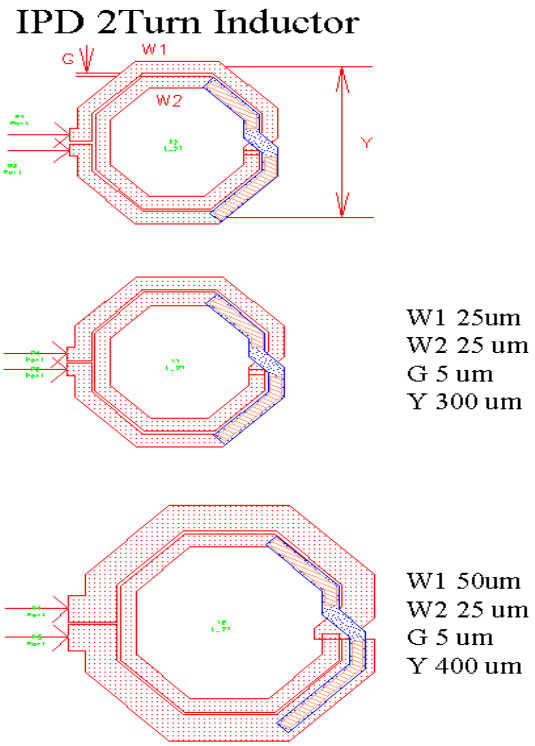

Figure 7 Typical IPD Mechanical Object

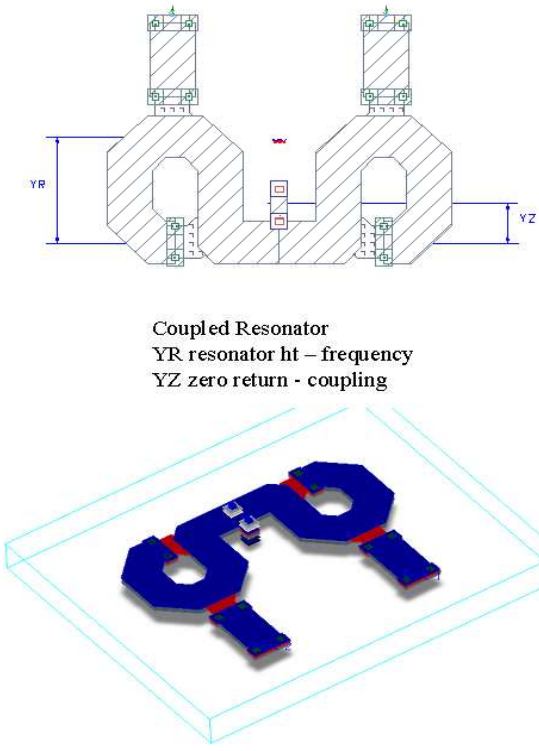

Figure 8 Typical LTCC Mechanical Object

It should be noted that at this stage the mechanical objects do not have a direct link to the material properties, nor to the vertical stack of the particular technology and supplier that is to be used. These objects can therefore be re-used if a design is transferred between 2 suppliers. Objects having similar electrical functions in different technologies have been created. This allows a design carried out using one technology to be transferred to another (For example LTCC to IPD or vice versa).

Furthermore the creation of new mechanical objects is quite straightforward so that new novel designs can be created by this methodology.

The second step in the design process is to couple the technology file for the target process to the mechanical objects. A series of batch based electromagnetic simulations of the mechanical objects within the desired technology file framework creates data for a look-up table based model for each component (L, C or more complex resonator element).

This process is very easy to repeat with a new technology file, facilitating design transfer between suppliers and technologies. Figure 9 shows the schematic image of the LTCC coupled line resonator of Figure 8.

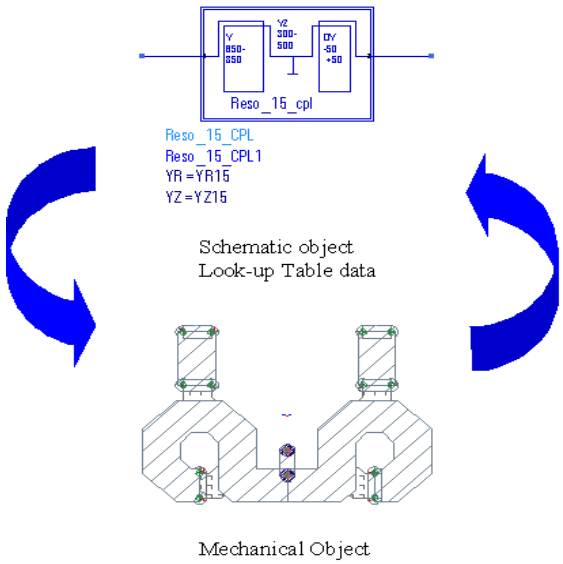

Figure 9 Schematic Object Linked to Mechanical Object

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Closed Loop EM design

The process described above allows for the creation of a set of project and technology related schematic objects that can be optimized to produce the required RF functionality. Simulations using these models can be carried out in both the frequency domain and the time domain (Spice or Harmonic Balance).

At this level of the design, circuit optimization is carried out to determine the parameters of the schematic/mechanical object. This process is quite similar to that carried out in semiconductor design using library based objects that have electrical performance and create layout.

The next step of the process is to create complete sections of physical layout with the mechanical objects using the circuit optimization parameters.

A closed loop iterative process is used to obtain final layout that has the same electrical performance as the sum of the modelled portions. At this stage coupling effects between blocks are compensated for. This has the advantage of allowing the mechanical objects to be placed close together without any risk of causing unseen effects. This makes the designs created by this method more compact than those using a “P Cell” approach with large keep-out zones to avoid coupling.

Portability to Different Technology Files

As indicated above the design methodology naturally allows for portability between technology files. In order to re-design for an alternative supplier, using the same technology, the process employs the same mechanical objects with a new set of technology values. This process starts from the same basic schematic and simply re-optimizes the parameters of the objects to compensate for the new physical and mechanical parameters. The final EM close loop process is then carried out to create new layout for the new supplier.

In order to change from one technology to another, equivalent mechanical objects that have similar functions in both technologies have to be created. In this case the same basic schematic is used and the schematic/mechanical objects are swapped. Thereafter the process is similar to the normal design flow.

Design Portability

In order to illustrate the process 2 examples are given. The first case considers the transfer of a Bluetooth filter design between different LTCC suppliers.

The second case considers the transfer of a filter design between LTCC and IPD technology.

LTCC to LTCC supplier

In this example a 3 pole 1 zero filter that is designed for a Bluetooth module to fit under the active components has been designed using the methodology to operate with one LTTC foundry and has been successfully transferred to a second one.

The filter is designed using semi-distributed transmission line resonators with resonator coupling to create a suitable frequency zero in the response.

The 2 LTCC stacks are compared in Figure 10.

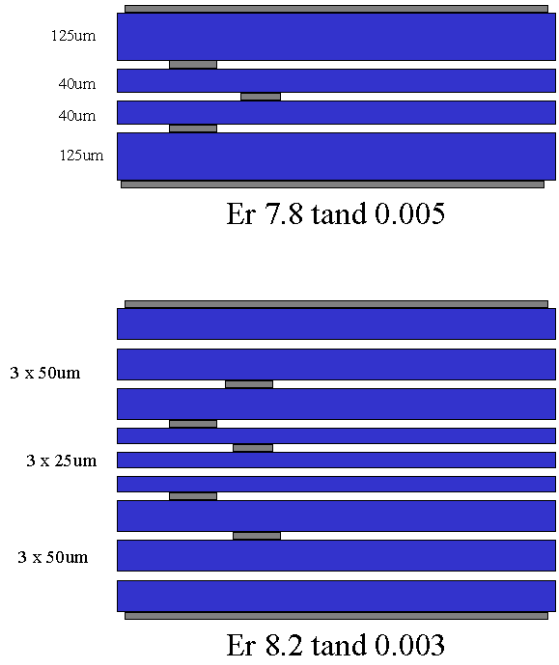

Figure 10 LTCC Stacks

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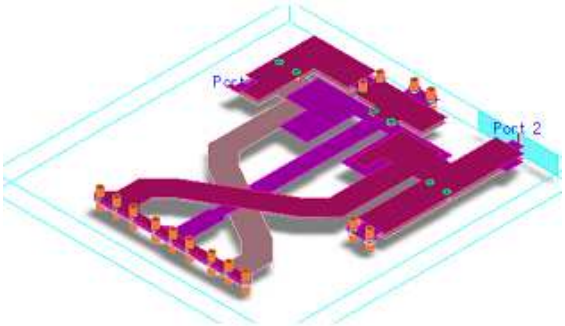
As can be seen the stacks and material properties of the 2 suppliers are quite unalike.

Despite this the mechanical objects were converted from one stack to the other and the design process completed rapidly.

The completed EM tuned filters for both stacks are compared in Figure 11.

Filter on Stack 1



Filter on Stack 2

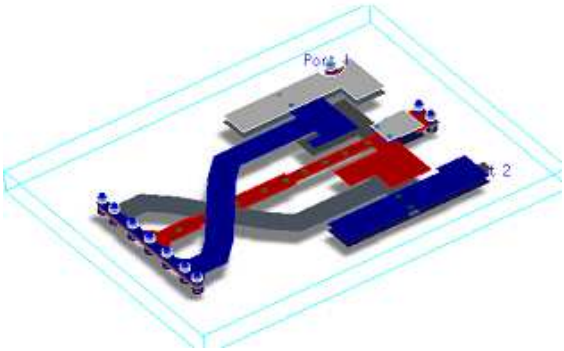


Figure 11 Comparison of full layout of filters

It can be noted that the 2 filters are quite similar but the physical dimensions of the filters are slightly different to compensate for the LTCC stack differences.

Electrical performance for both realisations was similar.

LTCC filter to IPD Filter

The above LTCC filter has also been transferred to an IPD technology. In this case the mechanical objects were quite different. The physical size of the standalone flip-chip filter is 2 x 2 mm compared to an LTCC size of 3 x 4 mm.

Figure 12 shows the preliminary outline drawing of the filter, whilst figure 13 shows the electrical performance.

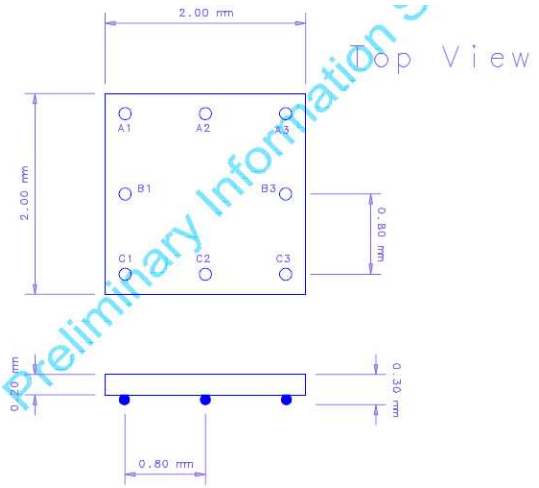


Figure 12 IPD layout

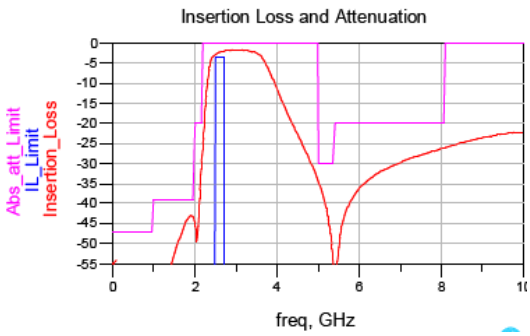


Figure 13 Electrical Performance

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Conclusions

This paper has shown the utility of a mechanical object based design methodology for buried functions within RF SiP. Portability between suppliers and between technologies has been demonstrated.

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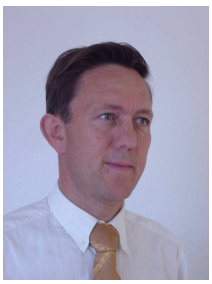
About the Author



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Prior to Insight SIP he was instrumental in setting up National Semiconductor's Design Centre in Sophia Antipolis.

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[1] Optimal design methodology for RF SiP from project inception to volume manufacturing, C Barratt, IMS2007 Workshop WSE System in Package Technologies for Cost, Size and Performance, Hawaii, June 2007.

[2] RF System in Package, design methodology and practical examples of highly integrated systems, C Barratt, IEEE Packaging Conference Como, Jan 2007.

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