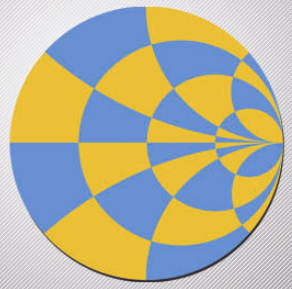


Insight SiP

System-in-Package (SiP) approach

ULTRA THIN RF SIP DESIGN

FOCUSSING ON AVAILABLE MASS MARKET TECHNOLOGY

CHRIS BARRATT, INSIGHT SIP
SOPHIA ANTIPOLIS, FRANCE

Agenda

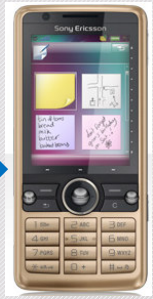
- Introduction
  - Nomadic Devices
  - Miniaturization
  - Thinner electronics
- Packaging Platforms for thin RF
  - Today – Heterogeneous mix of IPD, LTCC, Laminate, Flex
  - Tomorrow eWLP, RCP, Embedded die?
- Design Methodology
  - Technology File
  - Mechanical Objects
  - Closed Loop EM Design
- Design Examples
  - GSM 3G Transceiver
  - Ultra Thin GPS Solution
- Conclusions

Nomadic Devices

Mobile Phone

Motorola 1973

Smaller Better



2009

2009

2010 Intel MID

GPS Watch

1999

Smaller Better

2006

50mm dia 20mm thick

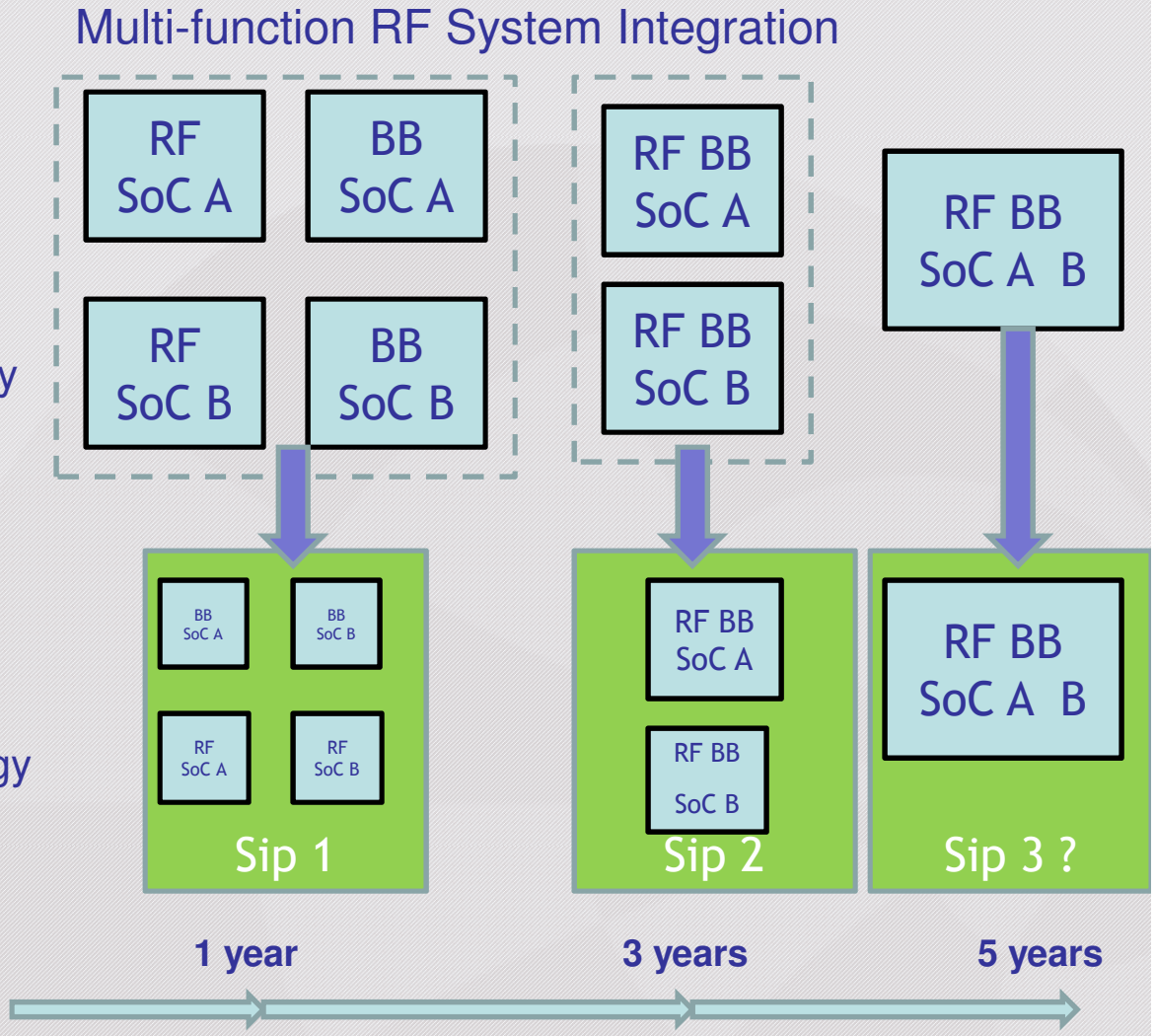
2009

Smaller Better

Real Watch?

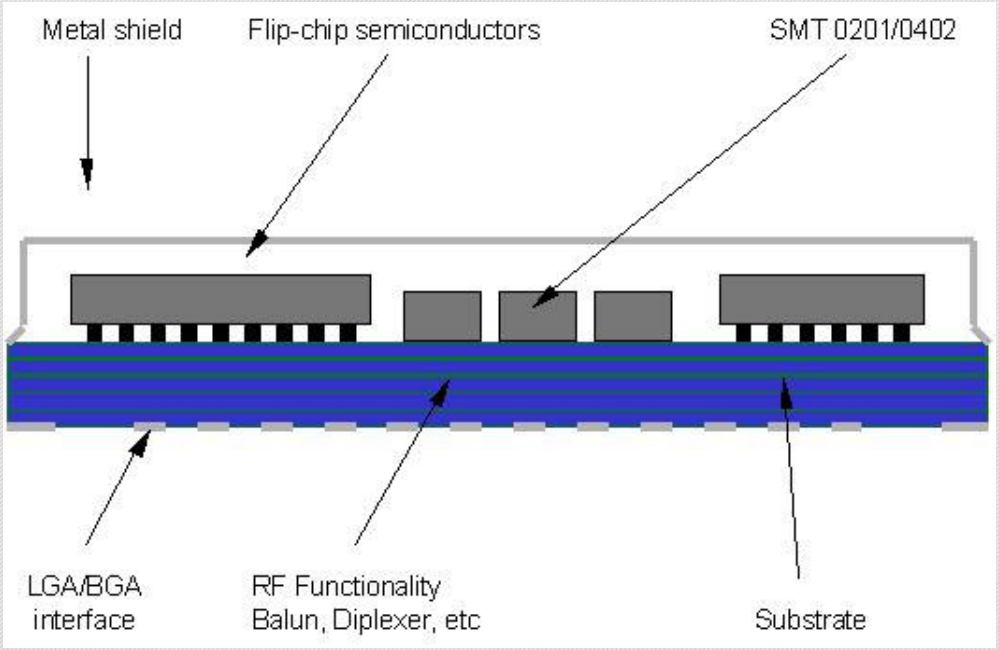
Miniaturisation X x Y

- System on Chip (SoC)
  - Long Design Period
  - High Risk
  - High Design Cost
  - Homogeneous Technology
  - Smallest Size
  - Lowest Production Cost
- System in Package (SiP)
  - Short Design Period
  - Low Risk
  - Low Design Cost
  - Heterogeneous Technology
    - Si, SiGe, GaAs,..
  - Slightly Larger Size
  - Low Production Cost



RF SiP

- RF SiP
  - Complimentary to SoC
  - Needed for nomadic devices with SoC
  - Allows Mix of Technologies
    - Si, SiGe, GaAs
  - SiP Technologies to match requirements
    - LTCC, IPD, Laminate
  - TSV, eWLP, RCP tomorrow?

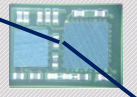


RF SiP Height Reduction

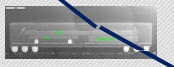
BT 2mm

WiFi 1.4 mm

GPS 1.3 mm



Stacked 2G/3G 1.2 mm



SiM card 0.8 mm

Z mm

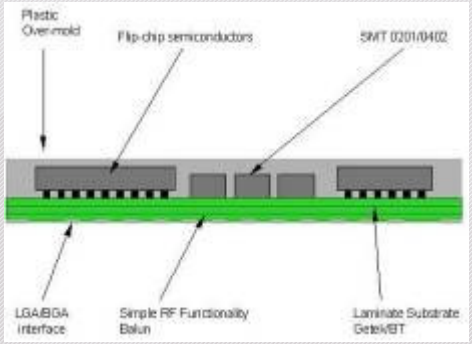
2

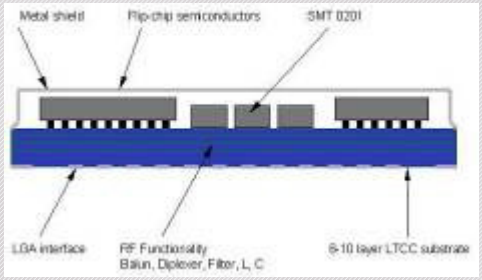
1

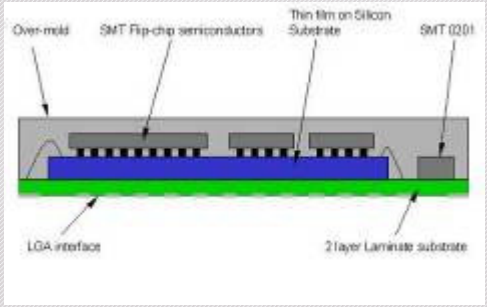
2001 2003 2005 2007 2009 Time

RF SiP Platforms

- Laminate based (εr 3 – 5)
  - 4 to 6 metal layers
  - Interco. RF Baluns in substrate
- LTCC based (εr 7 – 10)
  - 6 to 20 metal layers
  - Interco. RF baluns, Filters, matching in substrate
- IPD Glass or Si(εr 11.2)
  - 2 to 4 metal layers + doping
  - Interco. RF baluns, Filters, matching and high C in substrate

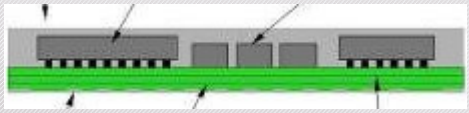






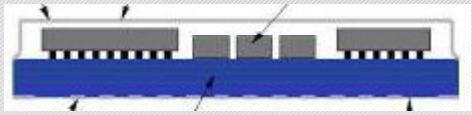
RF SiP Height Reduction

- Laminate
  - Reduce # & thickness layers 4L → 0.35 mm
  - Flip Chip Bumps → 0.1 mm
  - Thin die → 0.2 mm
  - Prefer LGA interface → 0
  - Use overmold (not shield) → 0.15 mm
  - Use only 0201 SMTs → 0.4 mm



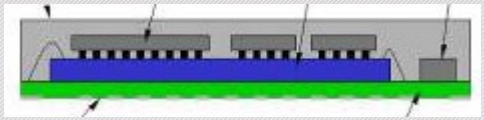
Min Ht 0.9 mm

- LTCC
  - Minimize thickness of substrate → 0.5 mm
  - Flip Chip Bumps → 0.1 mm
  - Thin die → 0.2 mm
  - LGA → 0
  - Overmold → 0.15 mm
  - No SMTs → 0
  - Interco. RF baluns, Filters, matching in substrate



Min Ht 0.95 mm with NO SMTS
Min Ht 1.05 mm with 0201s

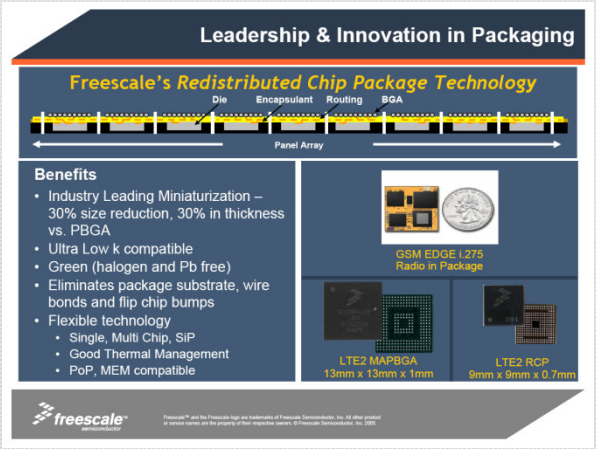
- Glass or Silicon Based (εr 11.2)
  - Use 2 layer flex for support → 0.1 mm
  - Thin IPD high density interconnect & dcpl → 0.15 mm
  - Flip Chip Bumps → 0.1 mm
  - Thin die → 0.2 mm
  - Overmold → 0.15 mm

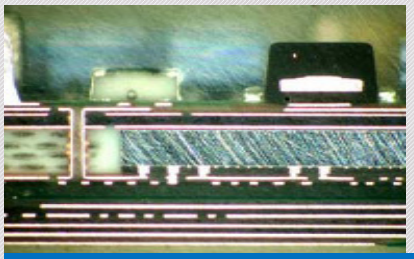


Min Ht 0.7 mm
SMT 0402 with no extra penalty

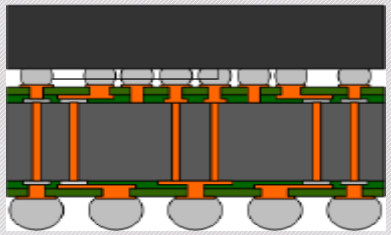
Further Thinning

- Freescale RCP
- eWLP
  - Imberra
  - Ibiden
  - Infineon
  - NXP
  - ASE
  - ….
- Stacked die with TSV





Casio Watch Module EWLP

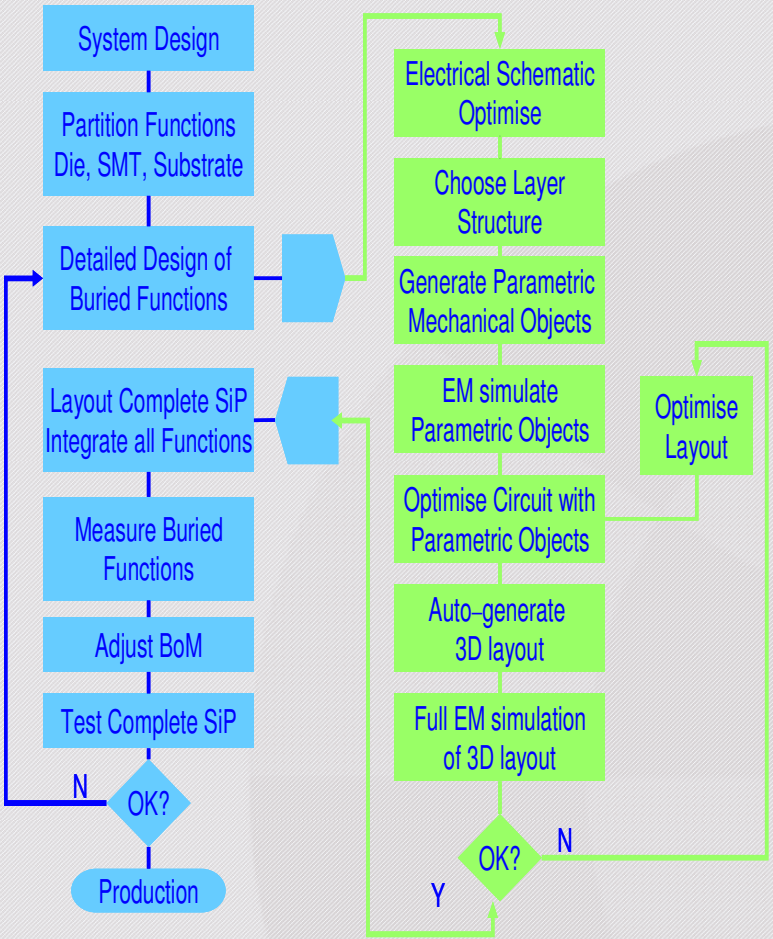


Stacked die with TSV

Lot's of good technology
Needs standardization
Cost control

RF SiP Design

SiP Layout and coupling

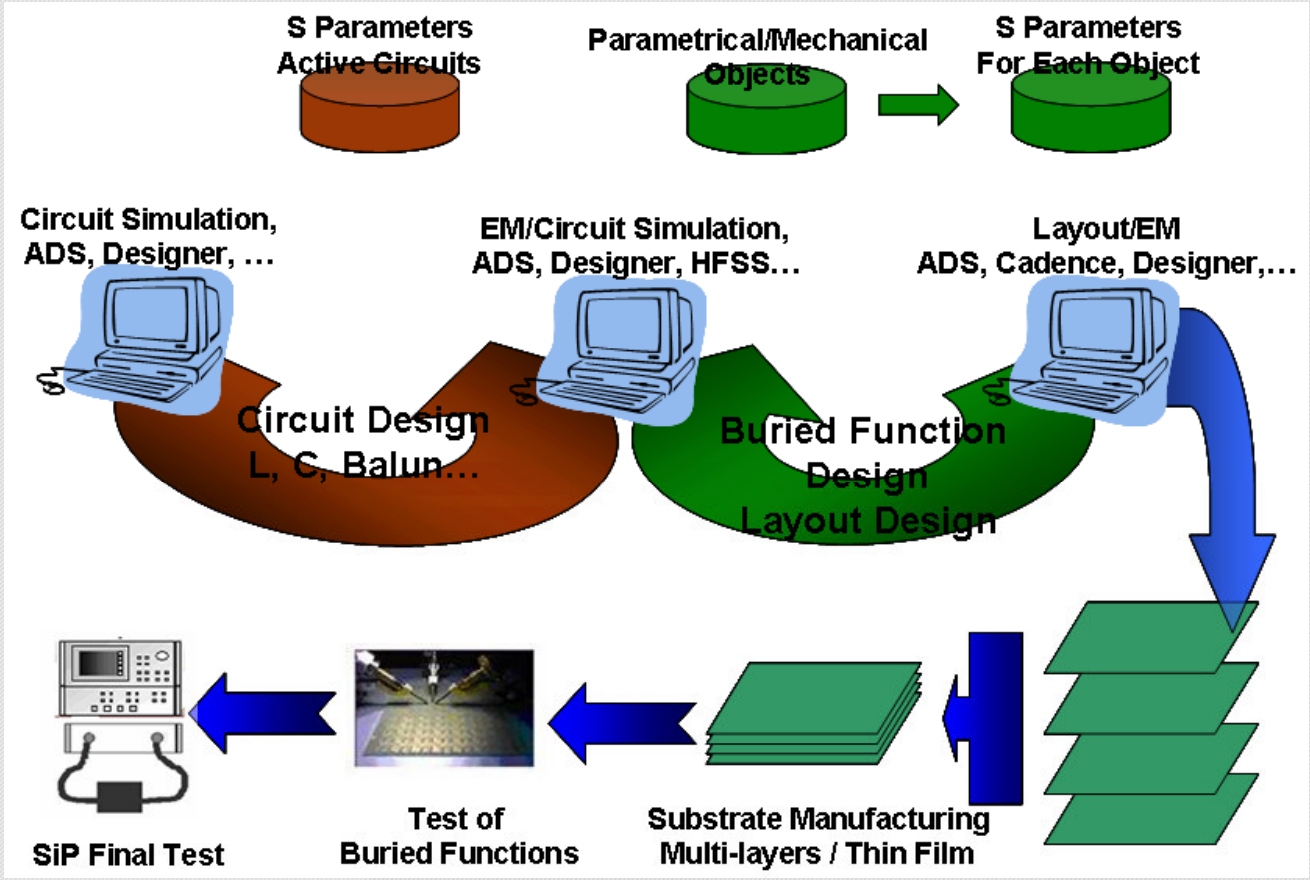


RF Function Design

Inside layers of RF SiP structure

IPD vertical in 2/3 layers
Laminate vertical structure

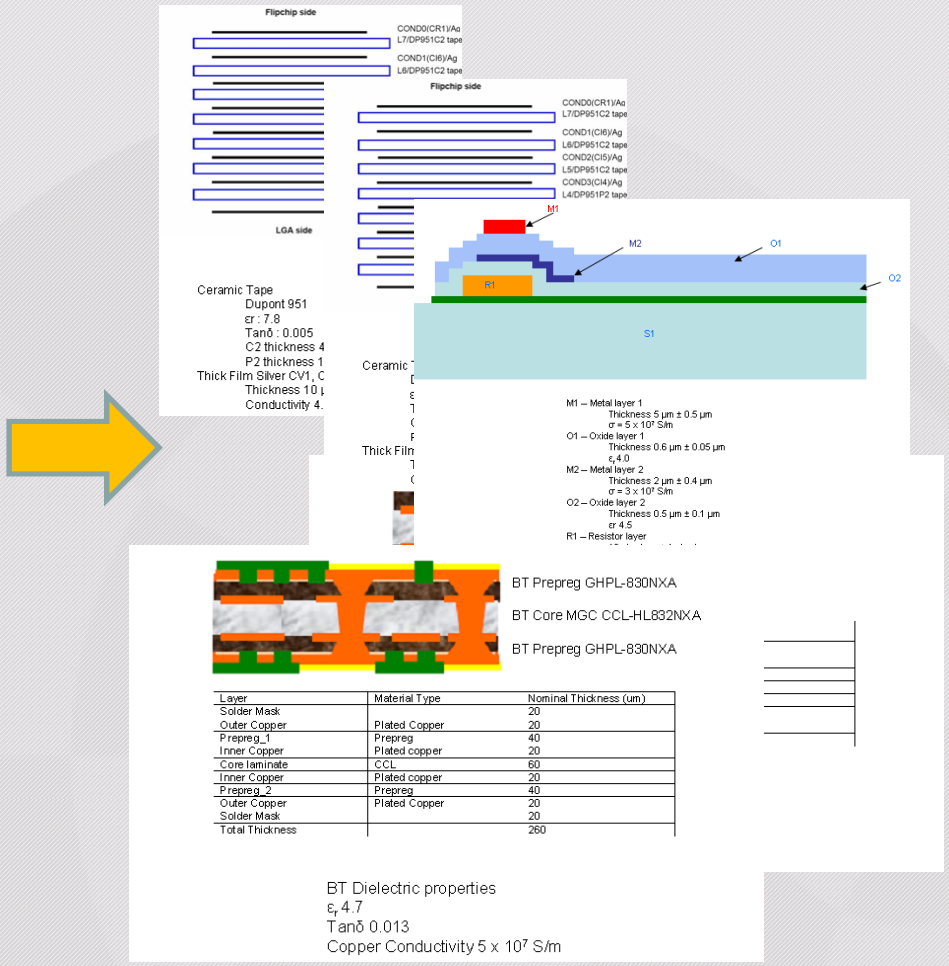
Design Tools



Based on multi-layer Electromagnetic Simulation coupled to Schematic level Simulation with S parameters

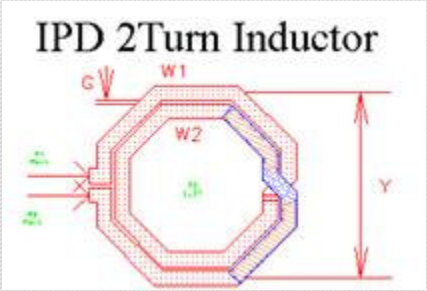
Technology Files

- Vertical Definition of Structure
  - Metal layers –
    - ➔Thickness
    - ➔Conductivity
  - Dielectric Layers
    - ➔Thickness
    - ➔Permittivity
    - ➔Loss Tangent
  - Relative position of layers
- Each Technology
  - Radically Different Technology file
- Each Supplier
  - Specific Technology file

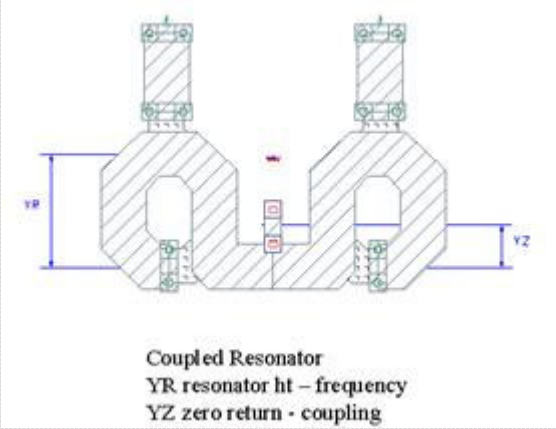


Mechanical Library

- Mechanical Objects
  - Multi-layer shapes
  - Controlled by mechanical parameters x, y, z,…
- Parametric Multi-layer Objects
  - Inductors
  - Capacitors
  - Resonators
  - Baluns
  - …..
- For each technology type
  - LTCC ➔ Multi-layer
  - IPD ➔ 2 – 3 layer fine resolution
  - Laminate ➔ mostly Ls and Baluns



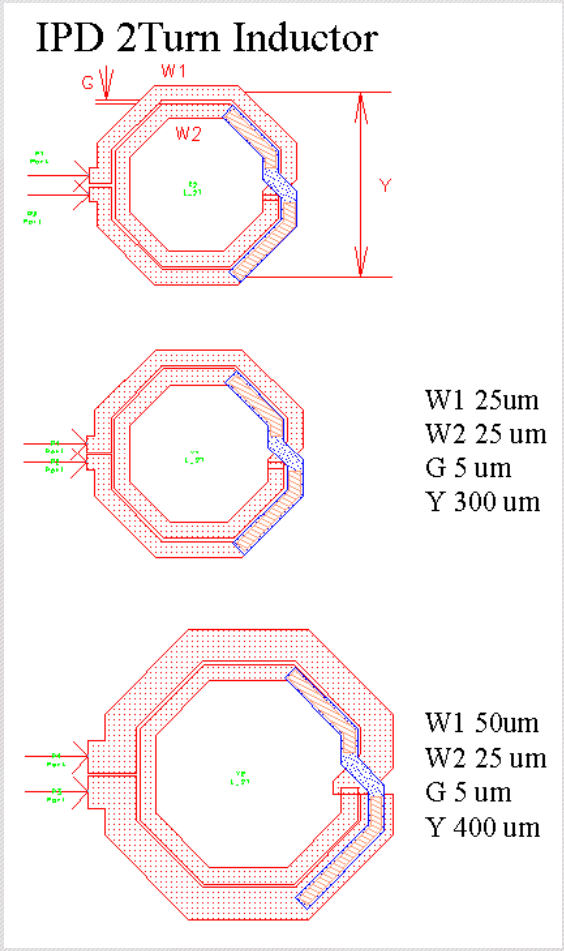
IPD inductor



LTCC Resonator

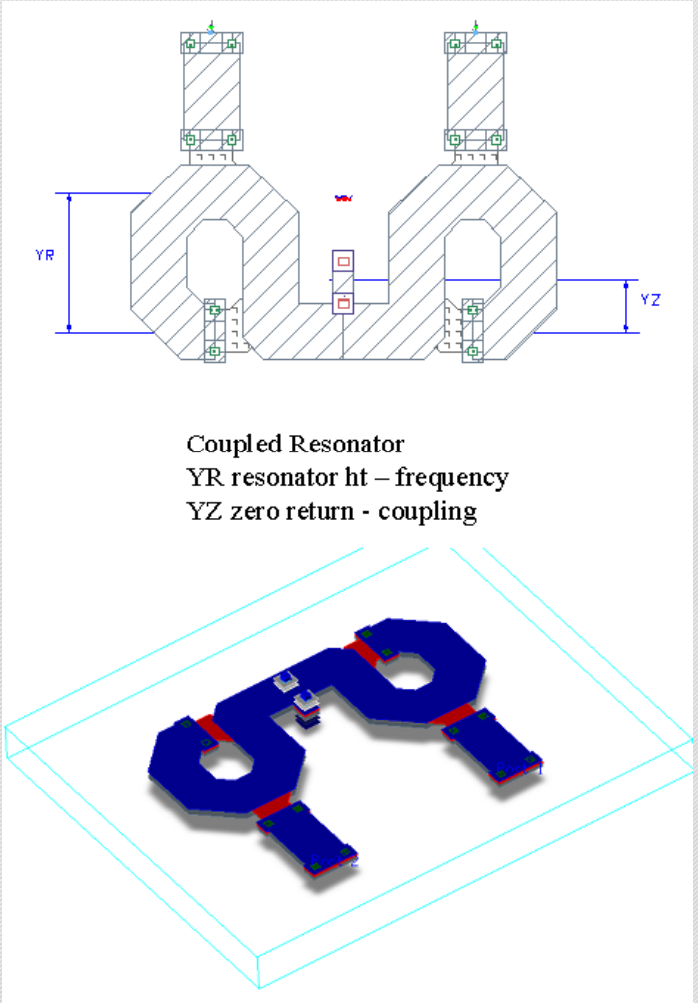
IPD 2 Turn Inductor

- 2 turn IPD inductor
  - Main Metal
    - use thicker lower loss metal
  - Crossovers on secondary metal
    - can be Al
- 4 mechanical parameters
  - W1 – width of outer winding
  - W2 – width of inner winding
  - G – gap between windings
  - Y – vertical dimension
- Can be mapped
  - To alternative metal types
  - To alternative substrates
  - To alternative dielectric thickness



LTCC 2 pole resonator

- Complex 2 pole resonator
- Folded line to reduce size
- Length controlled by vertical dimension
  - YR
- Zero position controlled by ground return via position
  - YZ

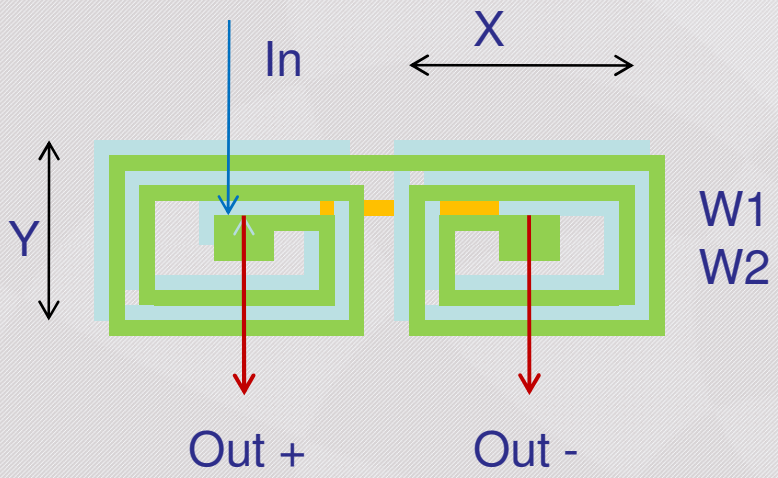


Laminate Balun

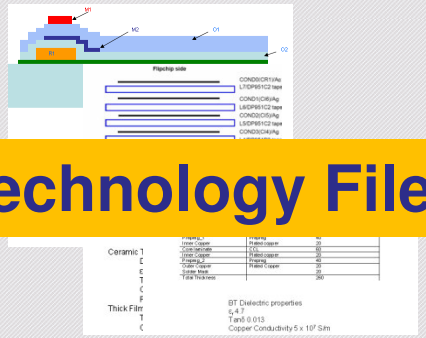
- Folded Balun
- Folded line to reduce size
- Uses 3 metal layers + 2 gnd layers
- Center Frequency controlled by
    - Length (X and Y parameters)
- Matching and Impedance

Transformation Ratio controlled by

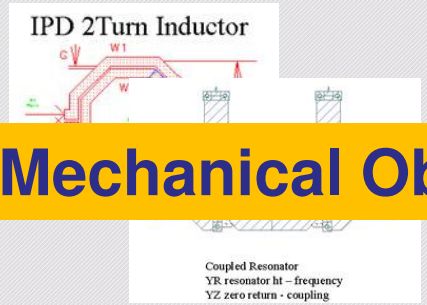
- W1 W2 and technology file



Schematic to Layout



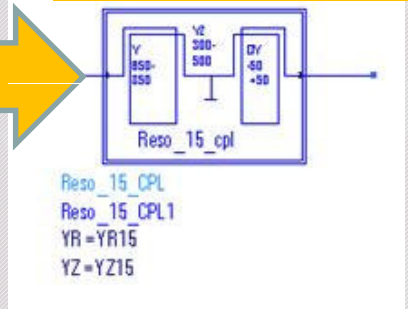
Technology File



Mechanical Object

Batch Mode
EM Simulation
Frequency
X, Y, Z,…

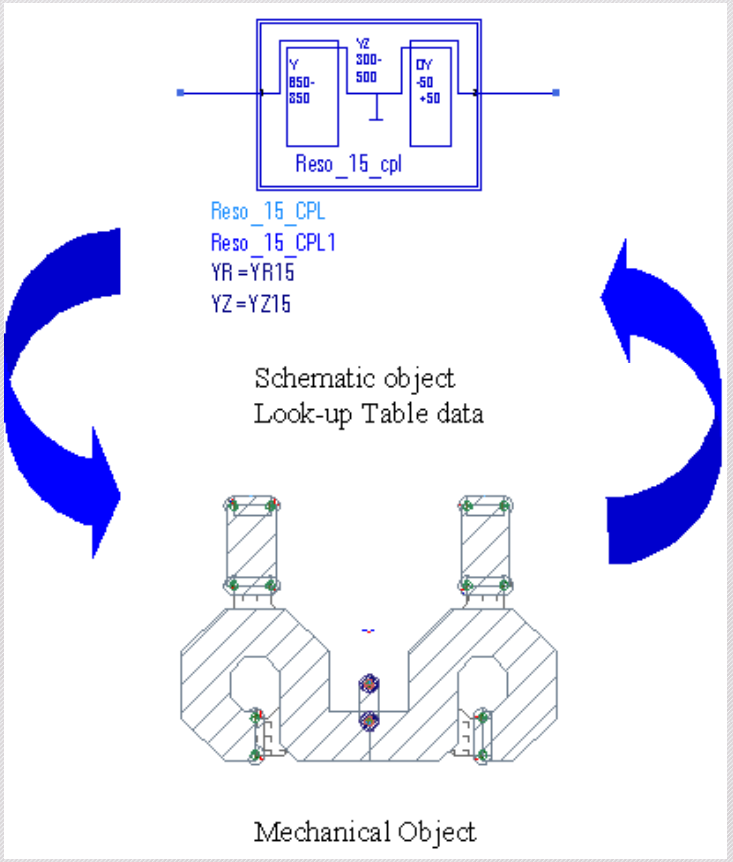
Schematic



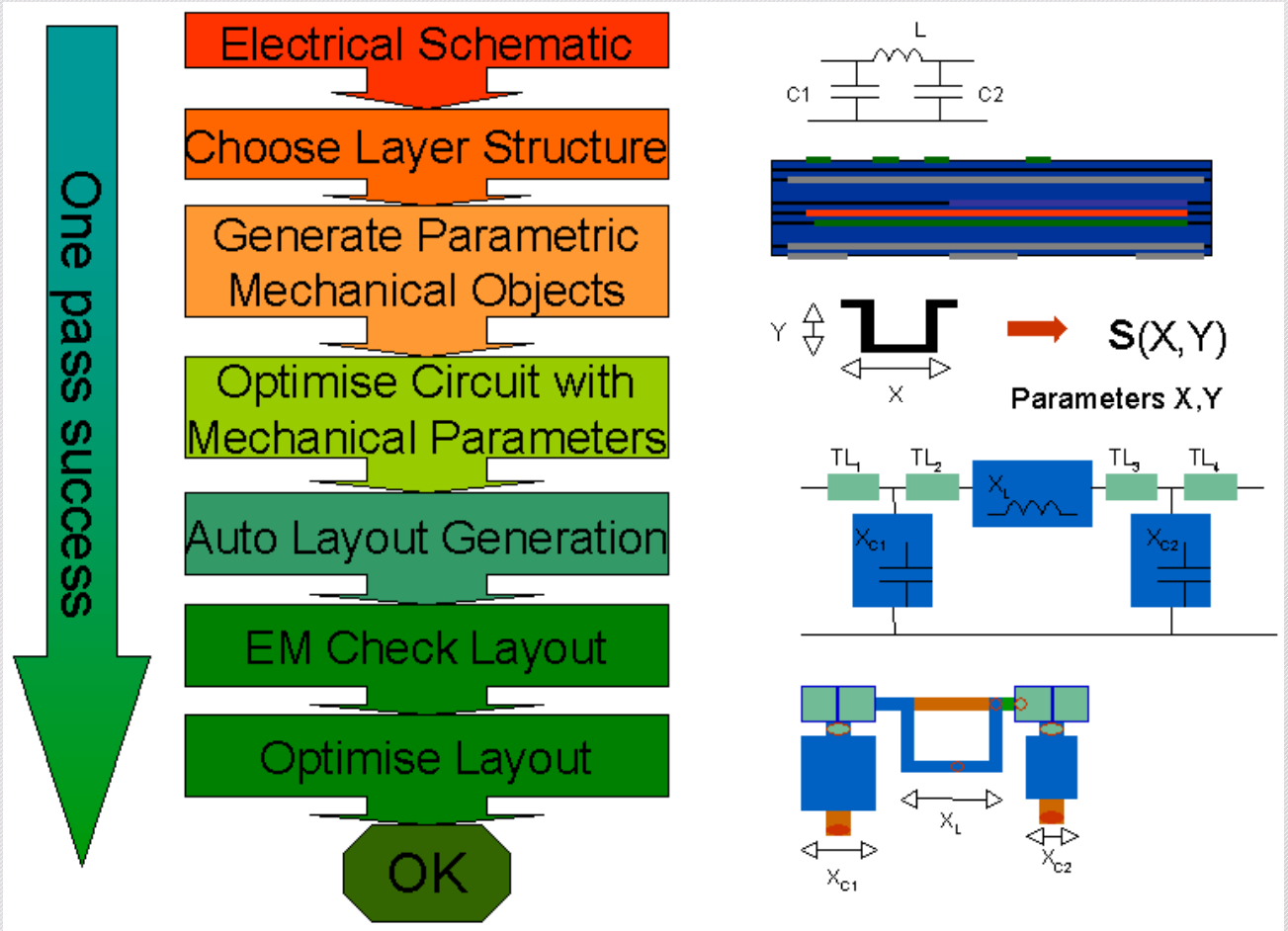
Electrical Model
of Mechanical Object
Within "Tech File" Environment

Schematic ⟷ Mechanical

- Library Created at Project level
- Mechanical Objects
  - Existing Library
  - New objects for project (Creativity)
- Schematic Object
  - Based on Tech File + Mech. Object
  - EM simulation based
  - Captures all local parasitics
- Changes in Technology
  - Re-spin EM simulations
  - Use new Tech File



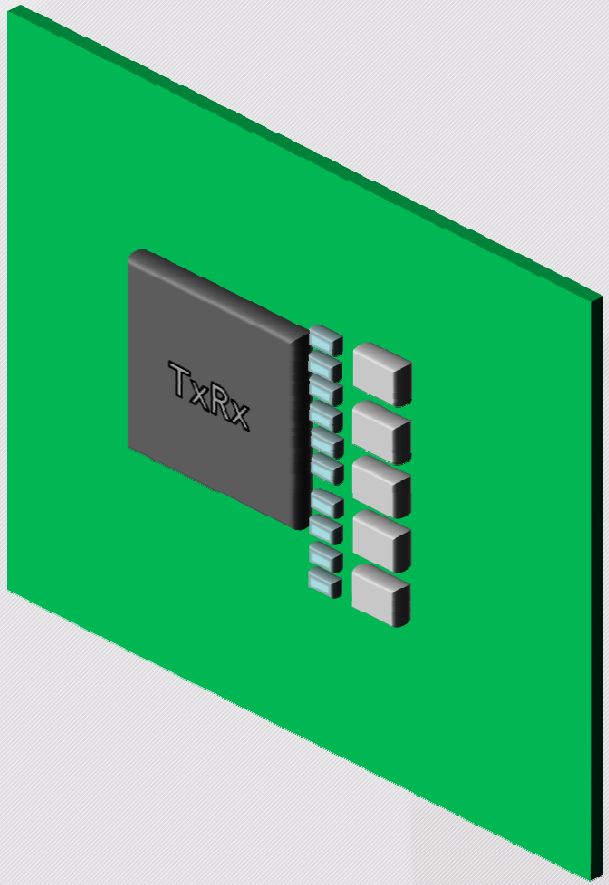
Closed Loop EM Design



Design Examples

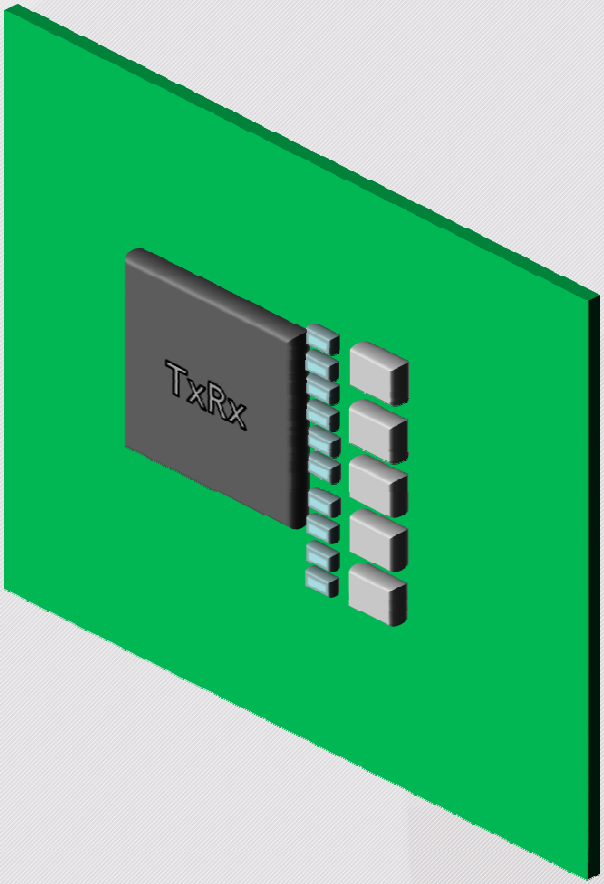
- 2G/3G Transceiver
  - Tx Baluns under die
  - 7 x 7 x 1.2 mm
- GPS 2 chip solutions
  - Laminate based
  - Full system with IPD

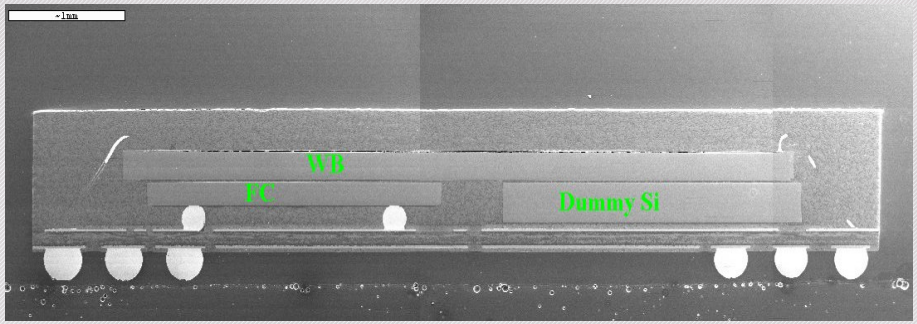
2G/3G Transceiver



Tx Side - 5 Baluns and 5 matching networks

2G/3G Transceiver

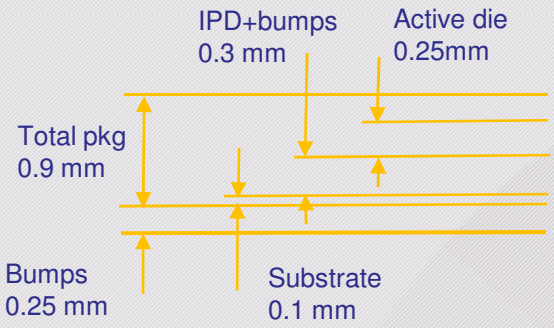


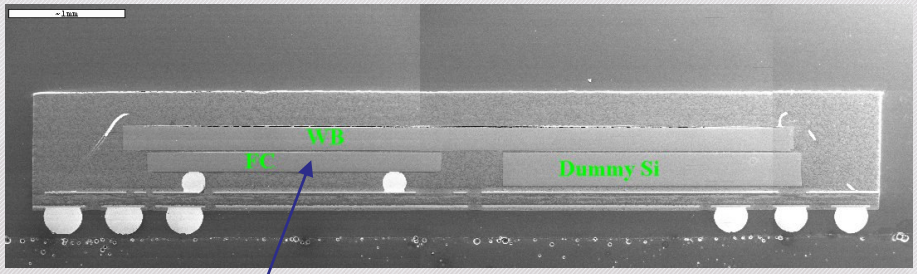


Tx Side - 5 Baluns
and 5 matching networks

All baluns integrated in IPD under active die in package

2G/3G Transceiver



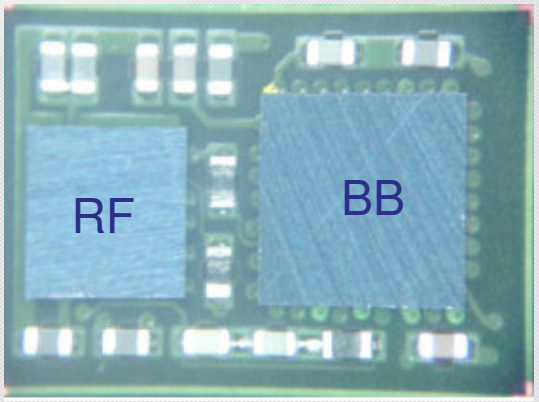


5 channel Baluns + Matching using EM based design methods
Wire bonds and Ground plane interaction included in model
➔First pass design success ➔ **1.2 mm Height**
Ultimate thinning ➔

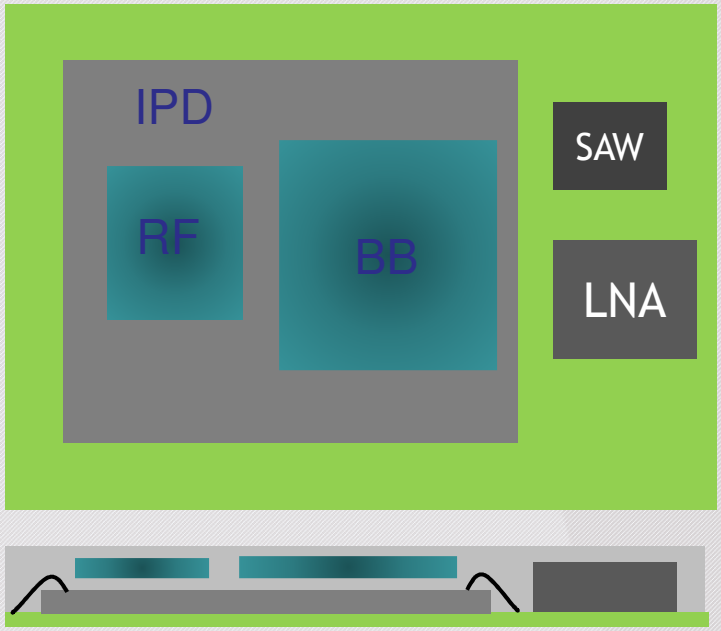
Active die	ca 0.15 mm
Bumped IPD	ca 0.25 mm
Wire bond overhead	ca 0.25 mm
BGA bumps	ca 0.15mm

➔ **0.8 mm**

GPS Examples



Substrate 4L	0.4mm
FC die	0.35 mm
SMTs	0.35 mm
Overhead	0.1 mm
Bumps	0.15 mm
Total Height	**1 mm**



Substrate 2L	0.06 mm
IPD thinned	0.15 mm
FC Die	0.3 mm
LNA	0.4 mm
Overhead	0.1 mm
Total Height	**0.7 mm**

Conclusions

- Requirement for smaller and thinner solutions
- Current RF SiP Technologies and future trends
- Design methodology for RF SiP
  - Multiple technology platforms
  - Ensures first pass success for thin solutions
  - Takes care of coupling during design
- Examples
  - 2G/3G transceiver
  - GPS