Insight SiP

Recent Advances in RF SiP Designs

Chris Barratt

Insight SiP, Sophia Antipolis, France

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Outline

- RF SiP Why and When?
- RF SiP
  - Technologies
- Design Methodology
  - Initial Design Phase
  - Detailed Design Phase
- Examples
  - WLAN Modules
  - Integrated IQ Mixer
  - GPS Modules
  - Under the die integration

Motivation

- RF SiP is a road to get system solutions to market fast and at reasonable cost
- Optimized choice of SiP Technology gives lowest production costs
- The design methodology has to be:
  - Fast and accurate
  - Adaptable to all available technologies
  - Allow for maximum design creativity for new passive structures
- The design strategy is proven
  - for LTCC, Laminate and Thin Film IPD

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Pros & Cons

- Feasibility study is key to make best SiP choice
- Methodology gives close to first pass success for embedded passives (matching, filters, baluns,..)
- System related issues tend to be discovered during initial testing
  - Requires a pro-active approach to reduce digital/clock interference issues
- Design spins can be created by chip related issues that are discovered during SiP debug

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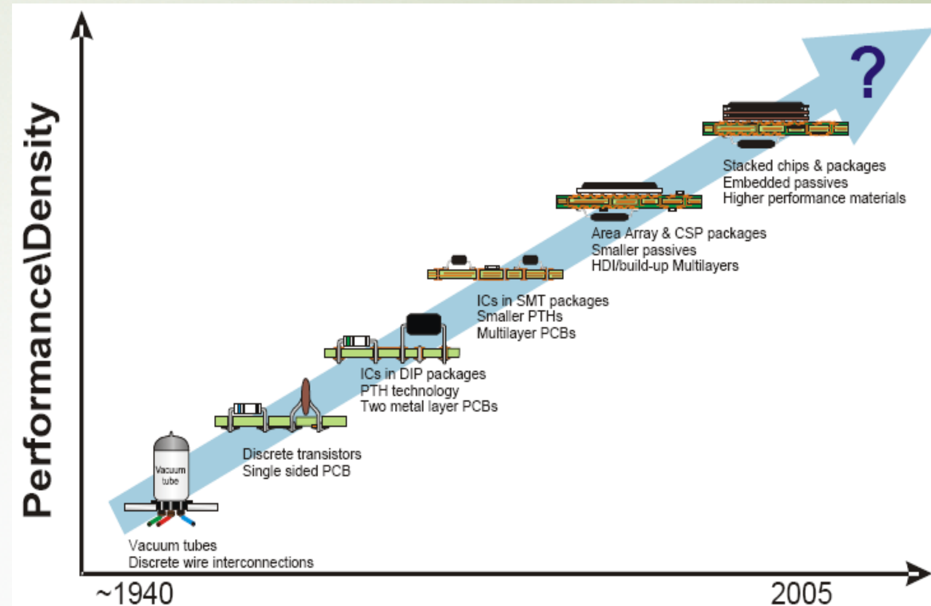
RF SiP Why and When

- Why to SiP
  - We need More than Moore
  - We need to prove system in market prior to developing SoC
- When to SiP
  - Early products
  - Products that need technology mix
  - Lower volume products



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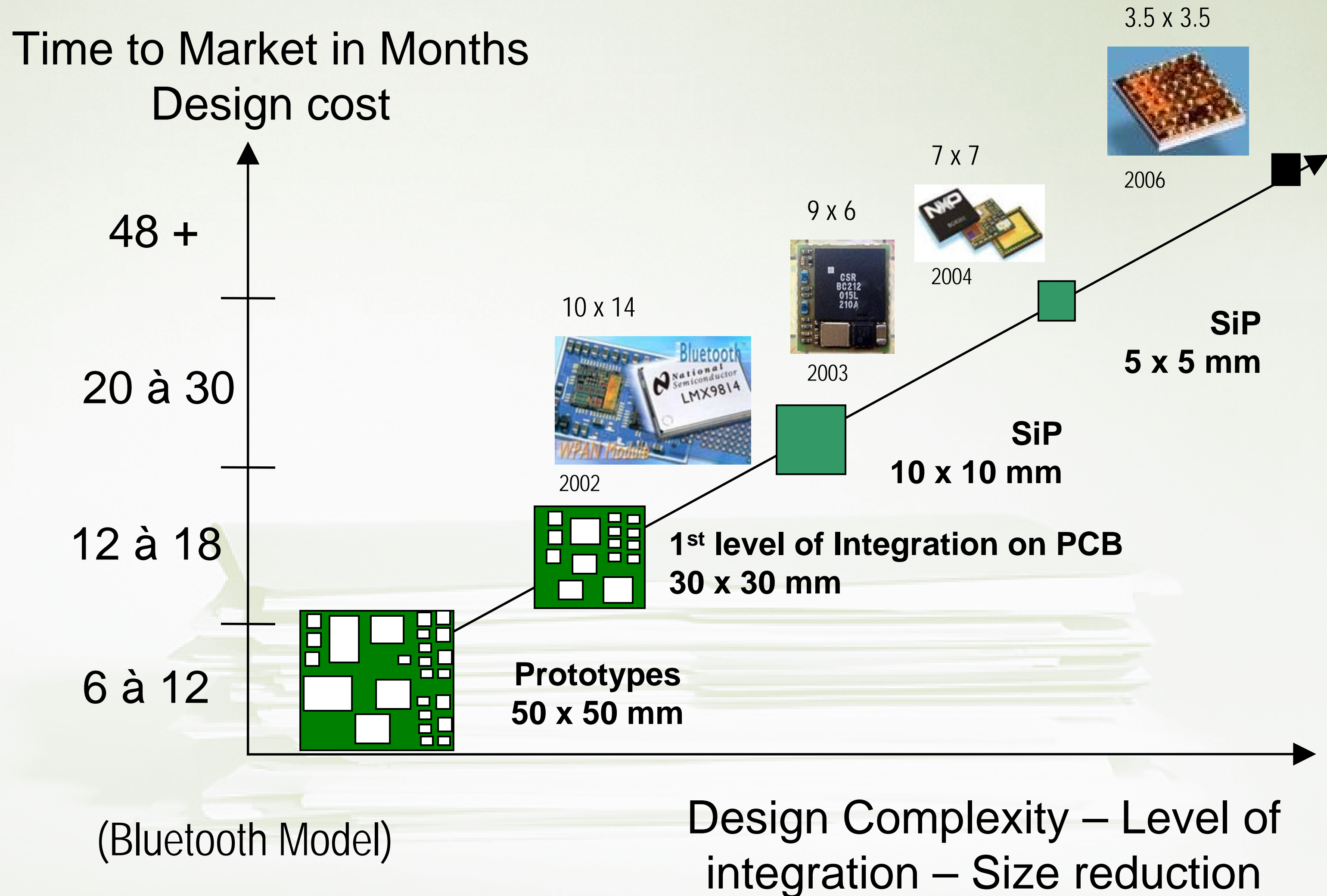
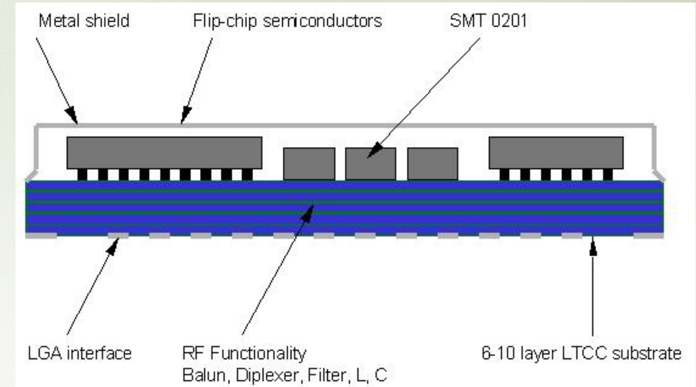
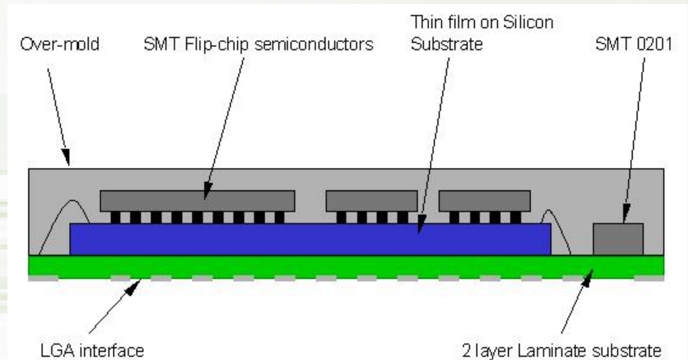
SiP life cycle



RF System in Package What is it?

- Complete 3D RF system
  - RF BB semi-conductors
  - SMT passives
  - Buried RF passives
  - Interface to application PCB (LGA, BGA)
- Fully self contained system
  - Tested
  - Semiconductor package format





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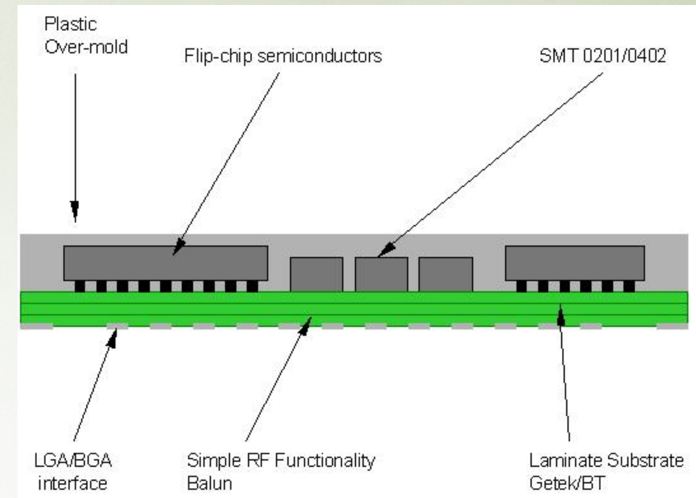
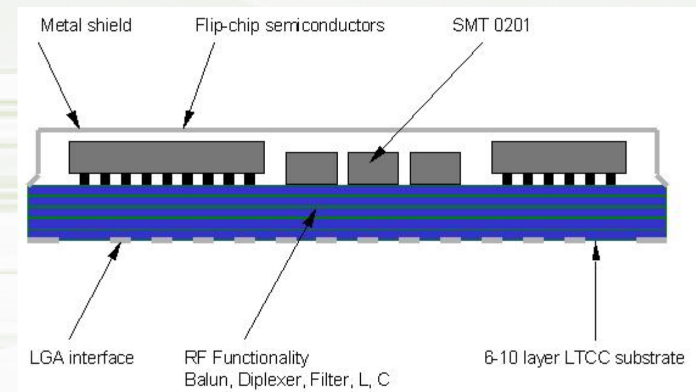
RF SiP Technologies

- Laminate based (ε_r 3 – 5)
  - 4 to 6 metal layers
  - Interco. RF Baluns in substrate
- LTCC based (ε_r 7 – 10)
  - 6 to 20 metal layers
  - Interco. RF baluns, Filters, matching in substrate





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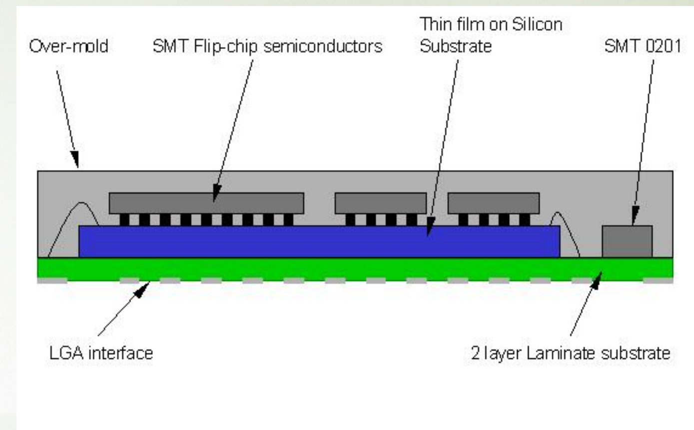
RF SiP Technologies

- Silicon Based (ε_r 11.2)
  - 2 to 4 metal layers + doping
  - Interco. RF baluns, Filters, matching and high C in substrate



SiP vs SoC

Parameter	SiP	SoC
Development Costs	x 1 Millions $	x 10 Millions $
Development Duration	12 to 15 months	more than 3 years
Time to market	1 yr	3 - 4 yrs
Technology mix	Yes Filters/Xtal	No
Typical size	5 x 5 x 1.4 mm	3 x 3 x 0.9 mm
Need for external components	No	Yes
Production costs	Low	Very low

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RF SiP Design

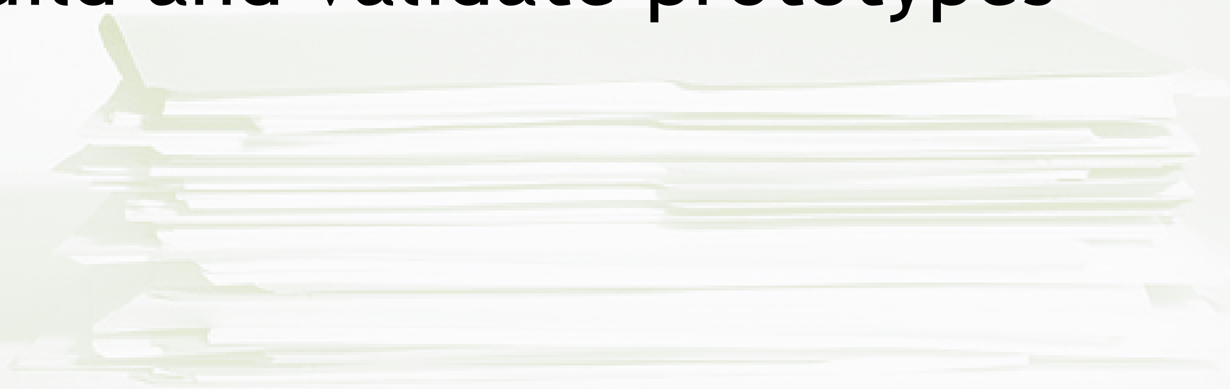
- Design for manufacture
  - Highly integrated (RF) systems and sub-systems
- System in Package approach
  - Multi-technologies : PCB, LTCC, Thin film, Thick film…
  - Emphasis on optimum overall cost in production
  - Use of “mature” non proprietary technologies available on the open market

RF SiP Design

- Initial Design & Feasibility
  - Determine tradeoffs
  - Select technology platform
  - Determine system partitioning

RF SiP Design

- Detail Design
  - Create and optimize schematic
  - Generate and validate layout and assembly
  - Build and validate prototypes



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Initial Design & Feasibility - Aim

- Chose System Architecture
  - Performances according to the Market Requirement,
  - Production and Development Costs,
  - Design to Production Lead Time.

Initial Design Feasibility - Method

- System partition
- Semiconductor Technology Choice : Si, GaAs, SiGe,…
- SiP Technology Choice : Laminate, LTCC, Silicon Based, Thin Film on Glass,…
- Assembly options (Flip-chip vs Bond-wires)
- Buried passives vs thin film passives vs SMT
- Compare SiP substrates
  - Size, Cost, NRE
- Compare Assembly options
  - Wire-bonding, Flip-chip, RDL, bumping, SMT,
- Compare test options

Initial Design Feasibility - Example

UWB Laminate Module

Description	Part #	Die size	Package dimensions		Component area	Courtyard Dimensions IPC7351		Courtyard area	Max Height	Quantity	*Total courtyard area*	*Total Component area*
			X	Y		X	Y					
Dimensions		mm x mm	*mm*	*mm*	*mm²*	*mm*	*mm*	*mm²*	*mm*		*mm²*	*mm²*
Actives												
RF + BB SoC	UWB_XX_100 Flip chip	5 x 5	5	5	25	5,5	5,5	30,25	0,5	1	*30,25*	*25*
Total Actives											*30,25*	*25*
RF Passive Functions												
3 to 5 GHz UWB Filter	Filter on top LTCC	3 x 4	2	4	8	3	5	15	0,6	1	*15*	*8*
Total RF passive functions											*15*	*8*
RF C, L												
Capacitors	<22pF		0,5	0,3	0,15	1,1	0,5	0,55	0,4	5	*2,75*	*1,1*
Inductors	<27nH		0,5	0,3	0,15	1,1	0,5	0,55	0,4	5	*2,75*	*1,1*
Total RF C,L											*5,5*	*2,2*
Crystal	NX2520SA 40MHz	2520	2	2,5	5	3	3,5	10,5	0,65	1	*10,5*	*5*
Total Crystals											*10,5*	*5*
Passives	0201 Capacitors Decou	C0201	0,5	0,3	0,15	1,1	0,5	0,55	0,4	10	*5,5*	*1,5*
	0402 Capacitors Decou	C0402	1	0,5	0,5	1,5	0,75	1,125	0,6	3	*3,375*	*1,5*
	0201 Inductors	L0201	0,5	0,3	0,15	1,1	0,5	0,55	0,4	0	*0*	*0*
	0201 Resistors	R0201	0,5	0,3	0,15	1,1	0,5	0,55	0,4	1	*0,55*	*0,15*
Total Passives											*9,425*	*3,15*
Maximum Height of components									**0,65**			
Total sum of courtyards											***70,675***	***43,35***
Estimated dimensions with 0.2mm kepout for overmold										**8**	**10**	

Overall Estimated Size

8 10 1,4

Item	Height estimation
	mm
Substrate	0,5
SMT solder thickness	0,05
Maximum Component Height	0,65
Overmold clearance	0,2
Overall Module Height	**1,4**

Initial Design Feasibility - Example

UWB Laminate Module

Description	Part #	Die size	Package dimensions X	Package dimensions Y
Dimensions		*mm x mm*	*mm*	*mm*
Actives				
RF + BB SoC	UWB_XX_100 Flip chip	5 x 5	5	5
Total Actives				
RF Passive Functions				
3 to 5 GHz UWB Filter	Filter on top LTCC	3 x 4	2	4
Total RF passive functions				
RF C, L				
Capacitors	<22pF		0,5	0,3
Inductors	<27nH		0,5	0,3
Total RF C,L				
Crystal	NX2520SA 40MHz	2520	2	2,5
Total Crystals				
Passives	0201 Capacitors Deco	C0201	0,5	0,3
	0402 Capacitors Deco	C0402	1	0,5
	0201 Inductors	L0201	0,5	0,3
	0201 Resistors	R0201	0,5	0,3
Total Passives				
Maximum Height of components				
Total sum of courtyards				
Estimated dimensions with 0.2mm kepout for overmold				

Overall Estimated Size

8 10 1,4

UWB SbSiP Module

Description	Part #	Die size	Package dimensions X	Package dimensions Y
Dimensions		mm x mm	*mm*	*mm*
Actives				
RF + BB SoC	UWB_XX_100 Flip chip	5 x 5	5	5
Total Actives				
RF Passive Functions in Passive silicon				
3 to 5 GHz UWB Filter	Filter on top of Silicon	2 x 3	2	3
Total RF passive functions				
RF C, L on silicon				
Capacitors 1nF/mm²	<22pF		0,15	0,15
Inductors	<27nH		0,3	0,3
Passives	100nF/mm²		0,5	0,5
Total RF C,L				
Total SBSiP substrate				
Size with 400um Bump ring				
Crystal	NX2520SA 40MHz	2520	2	2,5
Total Crystals				
	0402 Capacitors Deco	C0402	1	0,5
	0201 Inductors	L0201	0,5	0,3
	0201 Resistors	R0201	0,5	0,3
Total passives				
Maximum Height of components				
Total Laminate area				
Estimated dimensions with 0.2mm kepout for overmold				

Overall Estimated Size

8 9 1,4

UWB LTCC Module

Description	Part #	Die size	Package dimensions X	Package dimensions Y	Component area	Courtyard Dimensions IPC7351 X	Courtyard Dimensions IPC7351 Y	Courtyard area	Max Height	Quantity	*Total courtyard area*	*Total Component area*
Dimensions		mm x mm	*mm*	*mm*	*mm²*	*mm*	*mm*	*mm²*	*mm*		*mm²*	*mm²*
Actives												
RF + BB SoC	UWB_XX_100 Flip chip	5 x 5	5	5	25	5,5	5,5	30,25	0,5	1	30,25	25
Total Actives											30,25	25
RF Passive Functions												
3 to 5 GHz UWB Filter	Buried in LTCC					5	4	20	0	1	20	0
Total RF passive functions in LTCC buried layers											20	0
RF C, L buried in LTCC												
Capacitors	<22pF					1,5	1,5	2,25	0	5	11,25	
Inductors	<27nH					1,2	1,2	1,44	0	5	7,2	
Total RF C,L buried in LTCC											18,45	
Total use of internal LTCC layers											***38,45***	
Crystal	NX2520SA 40MHz	2520	2	2,5	5	3	3,5	10,5	0,65	1	10,5	5
Total Crystals											10,5	5
Passives	0201 Capacitors Decou	C0201	0,5	0,3	0,15	1,1	0,5	0,55	0,4	10	5,5	1,5
	0402 Capacitors Decou	C0402	1	0,5	0,5	1,5	0,75	1,125	0,6	3	3,375	1,5
	0201 Inductors	L0201	0,5	0,3	0,15	1,1	0,5	0,55	0,4	0	0	0
	0201 Resistors	R0201	0,5	0,3	0,15	1,1	0,5	0,55	0,4	1	0,55	0,15
Total Passives											9,425	3,15
Maximum Height of components									**0,65**			
Total sum of courtyards											**50,175**	**33,15**
Estimated dimensions with 0.2mm kepout for overmold										**7**	**8**	

Overall Estimated Size

7 8 1,4

Item	Height estimation
	mm
Substrate	0,5

- **SiP Comparison**
  - Substrate Size & Performances vs type
  - Assembly options
  - Cost & Time to Production

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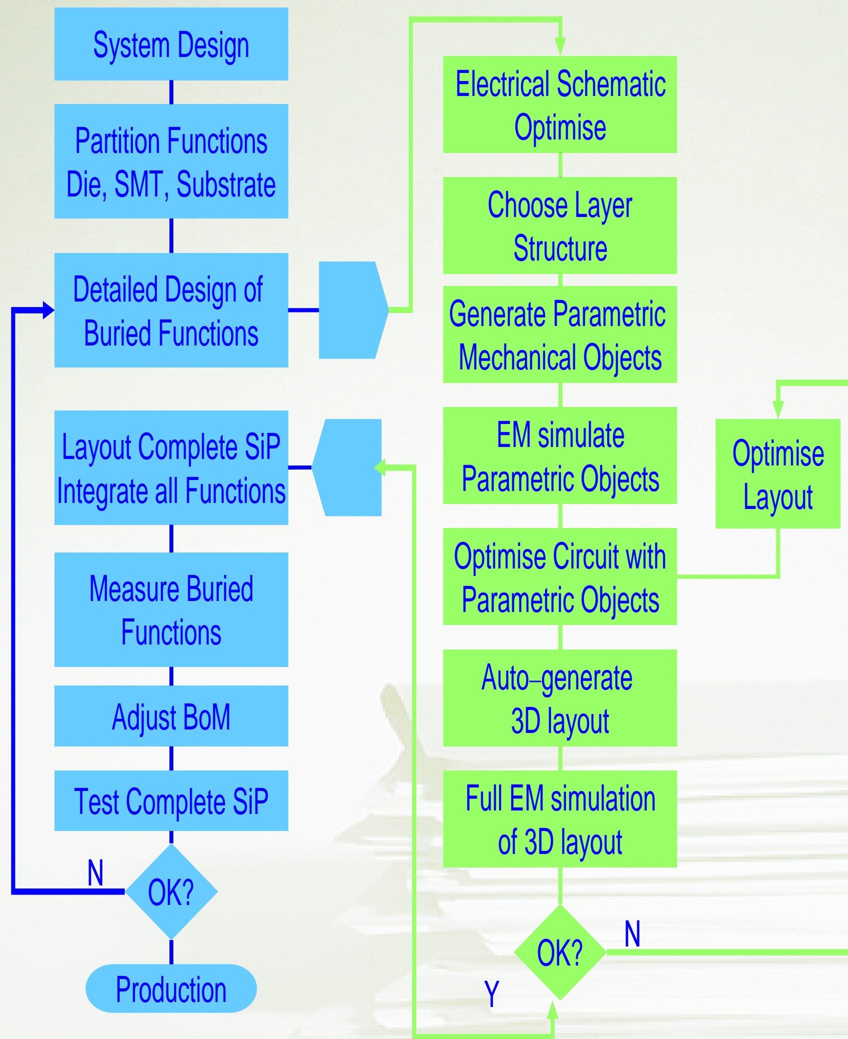
Detail Design



- **Standard EDA software based**
- **Flexible process no fixed libraries**
- **Step-by-step Process**

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Detail Design

- System model development
- Project-specific component library
- Circuit Optimization taking interactions into account
- Exhaustive simulation of electro-magnetic behavior
- Performance Optimization through electro-magnetic simulation feedback to circuit model.
- Proven two-pass success
  (with one-pass objective)

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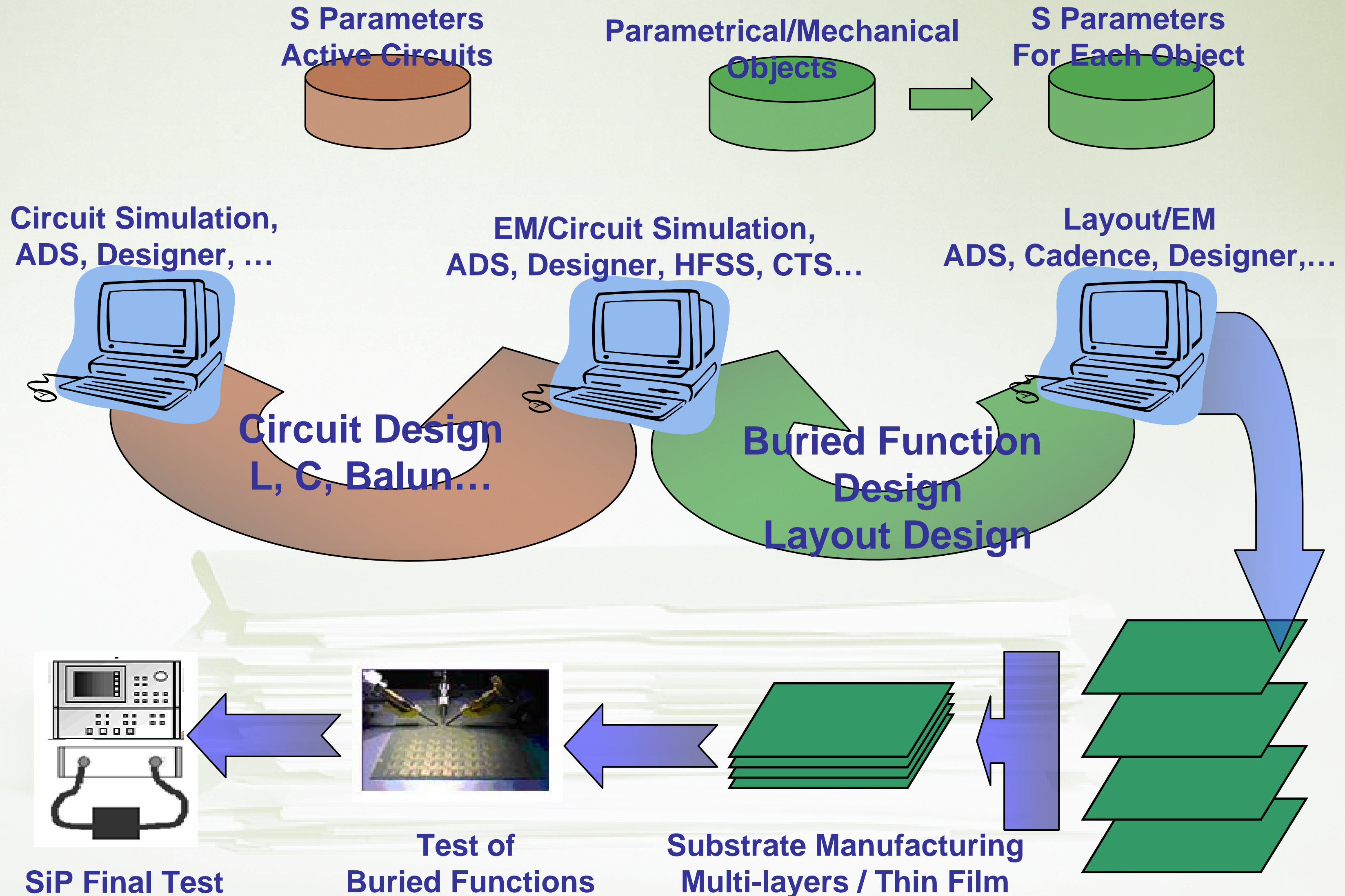
Detail Design EDA Tools



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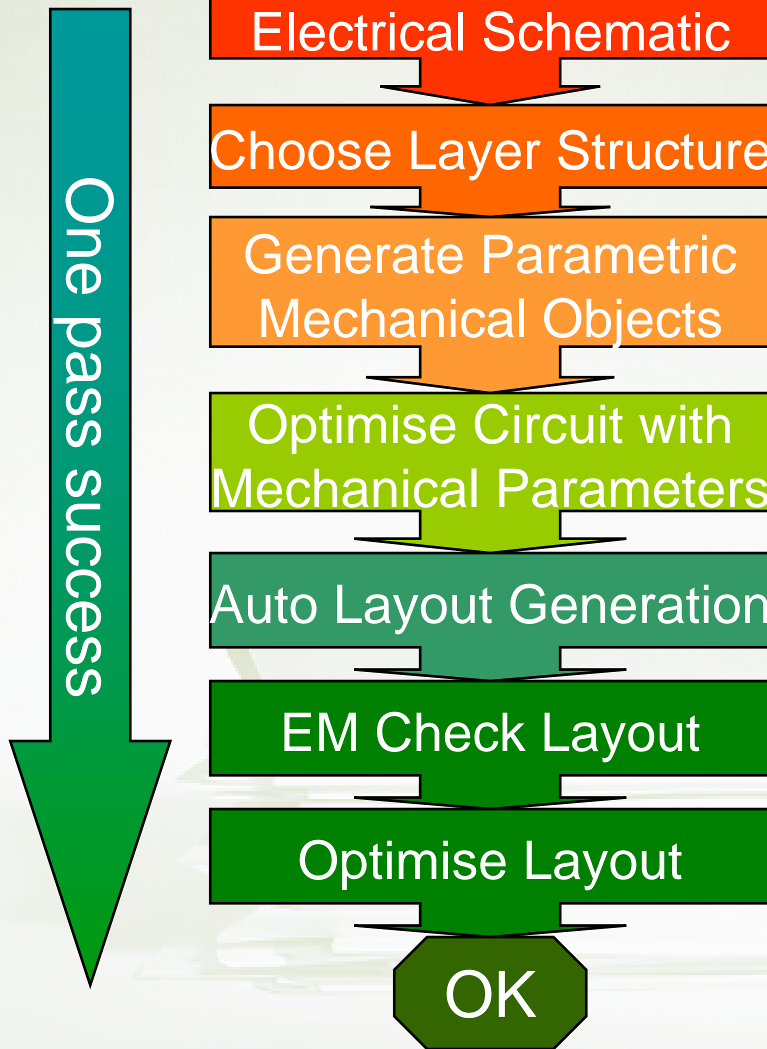
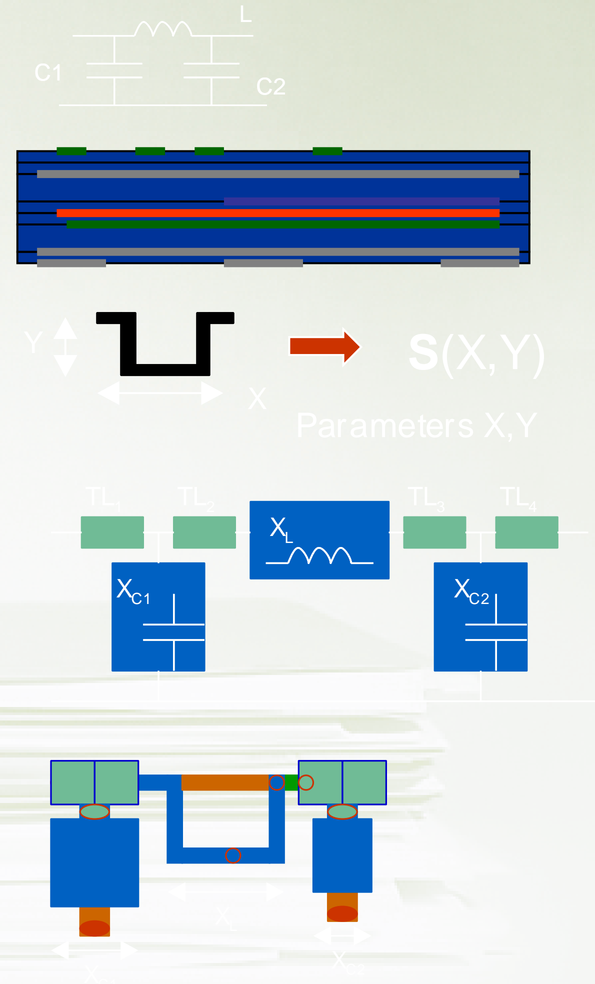
Design Flow for Buried Functions





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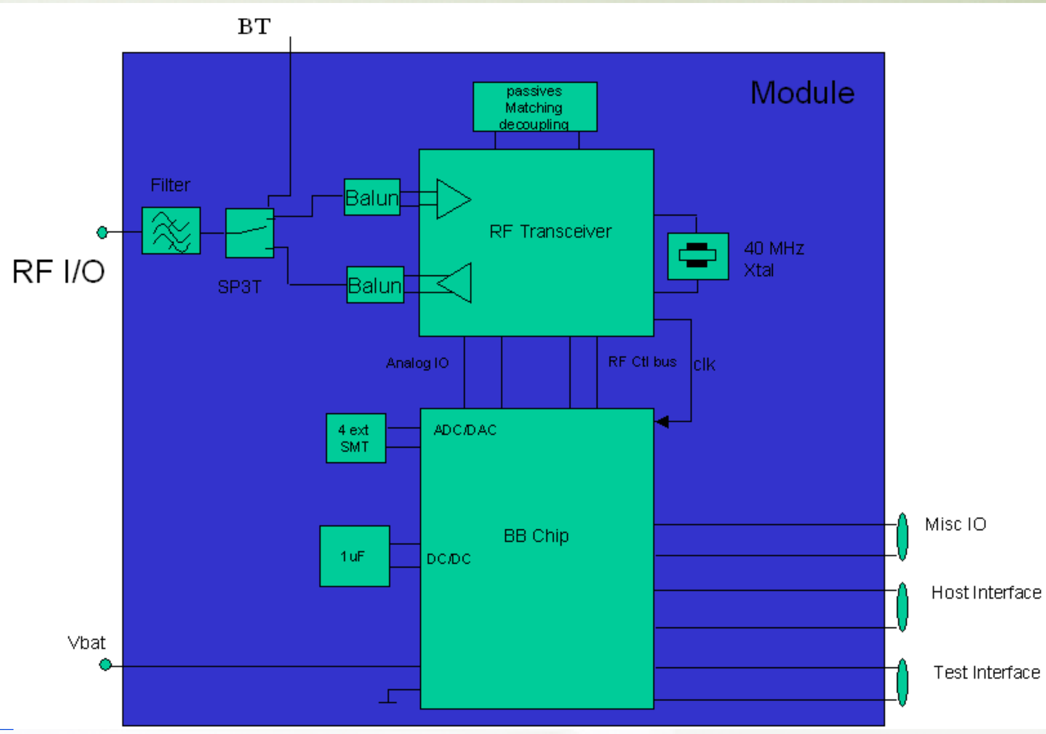
Examples

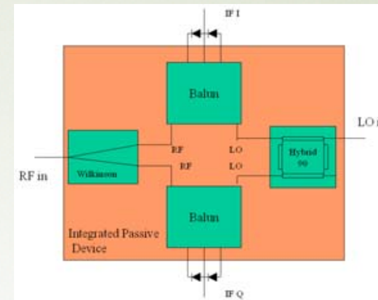
- WLAN Module 7 x 7 x 1.2 mm LTCC
- SiP based 433MHz FSK Radio
- GPS Modules Laminate and Silicon
- RF transceiver with Tx baluns

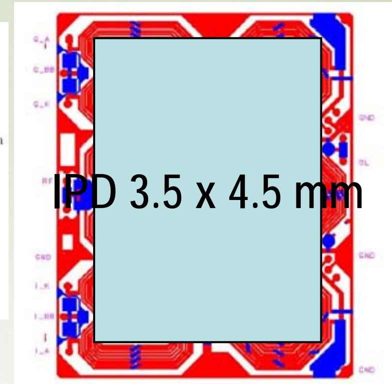
WLAN Module from Nanoradio

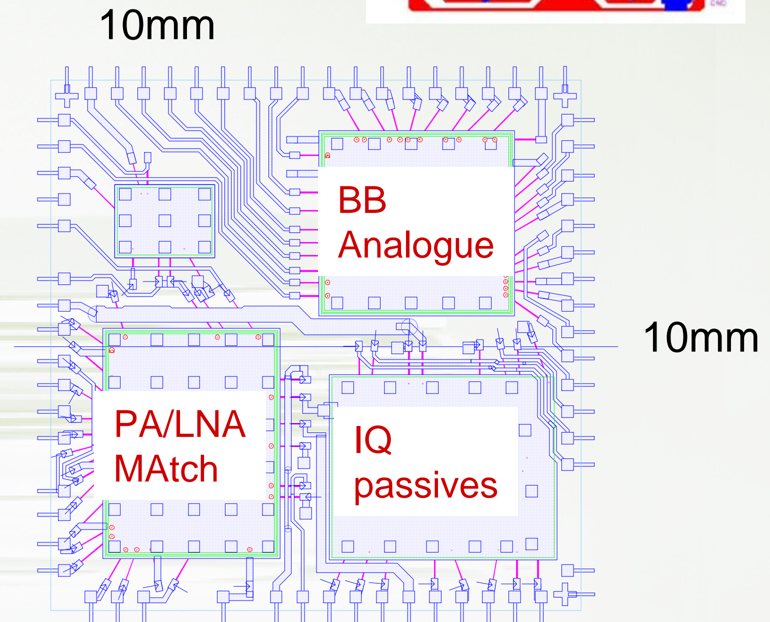


SiP for ISM FSK Radio

- Passive part of IQ mixer
- Passive part of PA and LNA matching
- Transmit ASIC
- Baseband Passives
  - Analogue filters (RC)
  - DAC resistor network

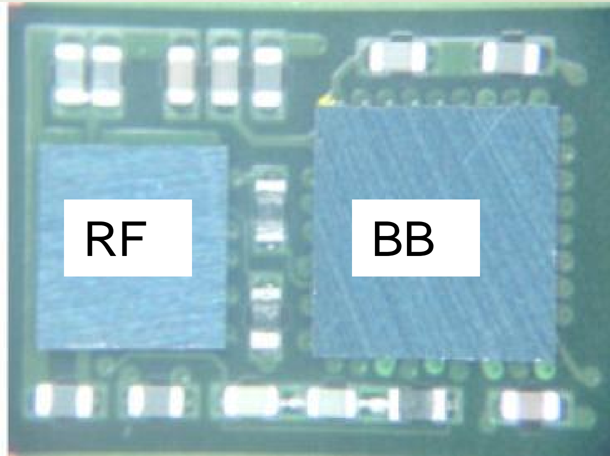


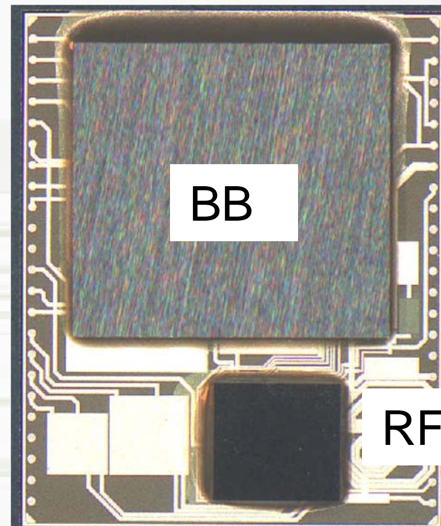




GPS

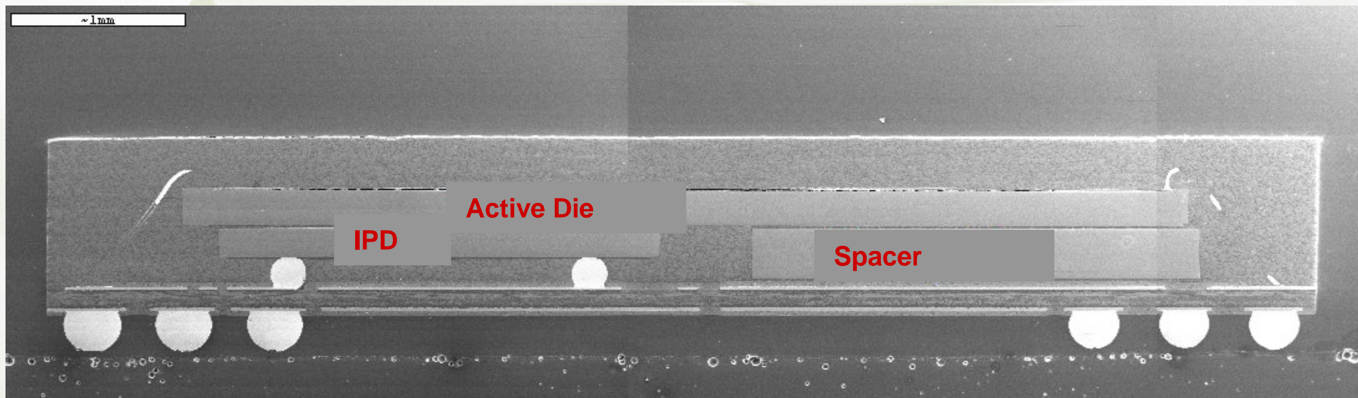
- Laminate based module
  - RF + BB
  - 6 x 4 x 1 mm
  - 4 layer laminate
  - EM simulation of coupling to optimise sensitivity
- IPD based module
  - RF + BB
  - Includes RF match
  - Chip to chip bumping
    - On bond pads for RF
  - Height < 0.5mm





RF Transceiver with Tx Baluns

- Initial design
  - BGA package + 5 ceramic baluns +25 SMTs
- IPD enhanced design
  - SAME BGA package
  - INCLUDES Tx Baluns
  - IPD is Flip chip under active die
  - Active die is wirebonded
  - IPD design includes Laminate and wirebond design



Conclusions

- RF SiP offers short time to market
- Feasibility allows choice of best technology
- Design process is under control
- Design process remains flexible
- Close to first pass design success